Five Level Diode-Clamped Voltage Source Converter for Custom Power Device Applications

N. Mithulananthan and P. Boonchiam*

Abstract—*Custom power devices are the importance to secure the sensitive loads from power quality problems. Especially in medium-voltage grids, the demand for securing larger loads has increased significantly. Installing of higher power levels leads to consider the multilevel converters with an increased number of levels and different topologies. Therefore, the five-level diode-clamped converter could be the interesting solution. This paper presents a method to allow a short-time stable operation of this topology without oversizing the DC-link capacitor and shows the drawback of this topology that its voltage levels are not stable for active power transmission and therefore the usage of this converter for custom power device applications. The voltage source converter is simulated in the power system using MATLAB program.*

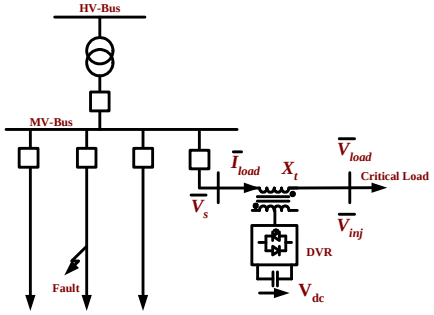
Keywords—**Custom Power Devices, Power Quality Problem, Voltage Sag/Swell, Multilevel Converter, Distribution of Electrical Energy.**

1. INTRODUCTION

Concerns on power quality problem have come into attention to many utilities and researchers for a decade. Many literatures devoted to obtain the methodology to find the way to prevent and relieve the power quality problem. The custom power had been proposed which concept of custom power and power electronic control in distribution areas by using the forced-commutation switches. It introduced the custom power solutions of power reliability rely on such novel components and systems as Solid State Circuit Breaker (SSCB) and distribution static compensator (D-STATCOM), Dynamic Voltage Restorer (DVR) and Unified Power Quality Conditioner (UPQC) [1-2].

Presently new systems for medium voltage grids with a compensation power of several MW are developed [3]. Even though several inverter topologies were already presented for custom power devices, the H-Bridge inverter is used in nearly all applications [4]. Going to higher power levels for compensating voltage disturbances in medium-voltage grids leads to the need of a series or parallel connection of devices or converters. One solution is a multilevel inverter with a high number of levels, especially the five-level diode-clamped inverter could be an interesting solution for this application. The main drawback of a five-level diode-clamped inverter is that it is not feasible for an active power transmission [5], because the capacitor voltage cannot be balanced for all four capacitors within the DC-link. Since delivering active power is essential in the custom power devices, a five-level diode-clamped converter seems not a suitable topology. However, the operation time of custom power device systems is quite short, therefore it may be possible to use different capacitances to make this inverter work properly. In this paper the derived equations will be explained and the needed capacitances will be calculated. Finally, these calculations will be verified with simulations of the designed system.

Fig. 1 shows the basic concept of custom power devices. For a successful compensation, the custom power devices must be able to detect voltage disturbances and control the converter to prevent against sags, swells, flicker, harmonic, etc.



(a) Dynamic Voltage Restorer

2. FIVE-LEVEL DIODE-CLAMPED VOLTAGE SOURCE CONVERTER

Main Circuit and Component

During the last 10 years, there has been steady growth multilevel converter topology as they can suit for the high voltage and high power applications. Multilevel VSC are the attractive technology for the medium voltage application, which includes power quality and power conditioning applications in the distribution system. The most well-known multilevel topologies

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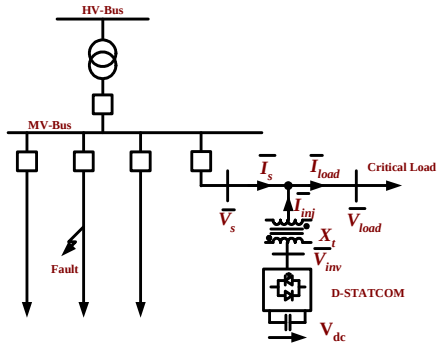
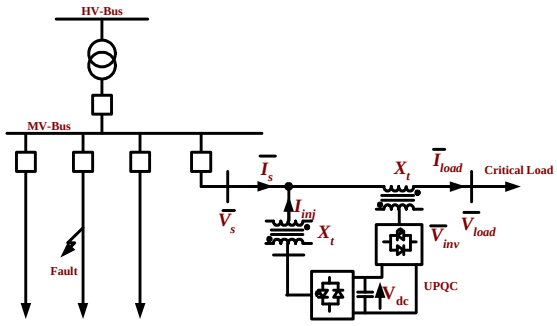
developed so far are shown in Fig. 2. There is diode-clamped multilevel voltage source converter.



(b) Distribution Static Compensator



(c) Unified Power Quality Conditioner

Fig.1 Simplified diagram of custom power devices connected between supply network and a critical plant

This multilevel topology can generate multilevel output voltages with low harmonics and reduce voltage stress on the power electronic devices. In order to compare the different multilevel topologies, a quantity called N_{index} is defined as given in Equation (1).

$$N_{index} = \frac{V_{dc,\max}}{V_{D,\max}} \quad (1)$$

where $V_{dc,\max}$ is the maximum dc bus voltage and $V_{D,\max}$ maximum nominal voltage requirement of the devices.

Fig. 2 depicts one leg circuit diagram of a five-level diode-clamped voltage source converter. This topology uses clamping diodes to limit dynamic and static overvoltages for switching devices. The clamping diodes are connected to taps of dc bus capacitor. In medium voltage grids, dc bus voltage is so high therefore capacitors are connected in series. Diode-clamped voltage source converter generates different voltage levels for output voltage in the ranging between positive and negative of $V_{dc}/2$. The number of levels N_{level} is

$$N_{level} = ceil(N_{index}) + 1 \quad (2)$$

The symbol *ceil*(x) represents the ceiling number of *x*. N_{index} is the number battery cell. The number of single capacitors N_C is

$$N_C = ceil(N_{index}) \quad (3)$$

and number of main switching devices is

$$N_{SW} = 2 \times ceil(N_{index}) \quad (4)$$

In contrast to main devices, the nominal voltage of the clamping diodes is higher than the voltage of one level. Therefore, it becomes necessary to place several diodes in series to achieve the required voltage. If rated voltage of a clamping diode equals rate voltage of the main switching devices, a N_{level}-level inverter leg needs the following number of clamping diodes.

$$N_{D,Clamp} = (N_{level} - 1)(N_{level} - 2) \quad (5)$$

For example, the five-level DC-VSC needs 4 capacitors, 6 diodes and 8 power switches. However, in practice, more diodes are needed due to the voltage derating of the series connection of up to (N_{level}-2) diodes. This fact introduces practical problems such as parasitic inductances or package difficulties.

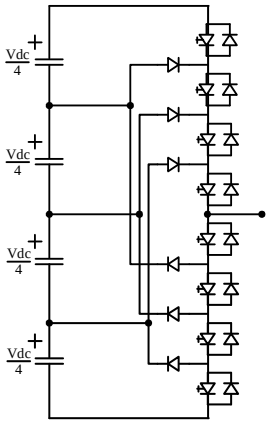


Fig. 2 One Phase Leg of a five-level topology

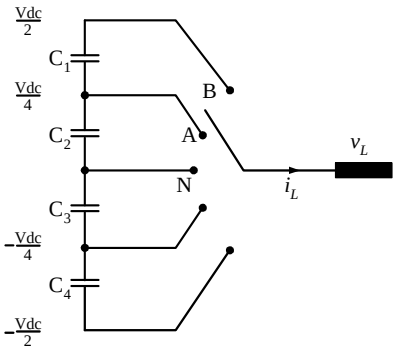


Fig. 3 Principle of a 5–level NPC

Switching Strategy

The most popular and simple switching schemes for the diode voltage source converter are step modulation and sine pulse width modulation (SPWM). Assume the magnitude of the reference sinusoid is 1.0. Comparing between triangular carrier waves and the references signal, this method calculates at switching states directly.

Each device is only switched twice per period Fig. 4 shows the switching principle for a five-level converter.

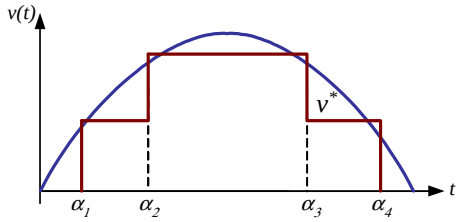


Fig. 4 Five-level step modulation switching strategy

The first level is turned-on at α_1 and the second level at α_2. To achieve a completely symmetrical switching scheme, the switch-off instances has to be

$$\alpha_3 = \frac{T}{2} - \alpha_2 \qquad \alpha_4 = \frac{T}{2} - \alpha_1 \tag{6}$$

And the switching times for the seconded half-period have to be delayed on T/2. The amplitudes of the fundamental sine-wave and the harmonics can be determined by a Fourier analysis. The decomposition of the function will be in the form

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left(a_n \cos(nx) + b_n \sin(nx) \right) \tag{7}$$

where

$$a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(x) \cos(nx)\, dx \tag{8}$$

$$a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(x) \sin(nx)\, dx \tag{9}$$

Because of the symmetry of the output signal, no a_n-coefficient exist and all even harmonics $b_{2k}, k \in N_0$ disappear. The fundamental amplitude b_1 can be found as:

$$b_1 = \frac{2}{\pi} \int_{\alpha_1}^{\pi - \alpha_1} f(x) \sin(x)\, dx = \frac{4}{\pi} \left(\cos(\alpha_1) + \cos(\alpha_2) \right) \times V_{DC} \tag{10}$$

Assuming V_{DC} the voltage of one level. B1 is depended on two variables α_1 and α_2 and has one degree of freedom. For example α_1 and α_2 can be chosen to minimize one specific harmonic. Depending on the demands of the electrical structure at the output of the converter, the 3rd or the 5th harmonics is chosen. The related Fourier-coefficients are

$$b_3 = \frac{1}{\pi} \int_{-\pi}^{\pi} f(x) \sin(3x)\, dx = \frac{4}{3\pi} \left(\cos(3\alpha_1) + \cos(3\alpha_2) \right) \times V_{DC} \tag{11}$$

In order to obtain the desired output magnitude and to minimize the desired harmonics, the following equation set has to be solved:

$$b_1(m_a) = m_a \times 2 \times V_{DC} \tag{12}$$

$$\frac{d}{d(\alpha_1, \alpha_2)} \times b_3 = 0 \tag{13}$$

The analytical solution of this nonlinear problem leads to piecewise linear functions over the entire modulation range. For minimizing the third harmonic, they will be

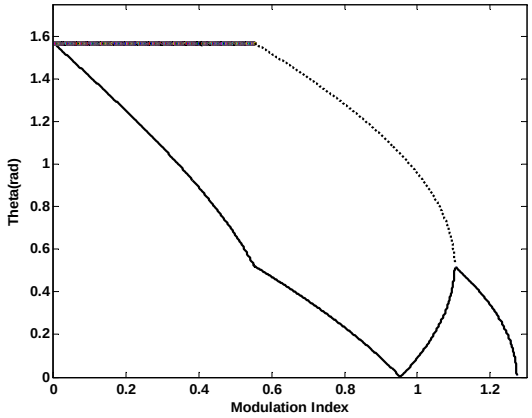


Fig. 5 Switching angles with minimizing the 3rd harmonics

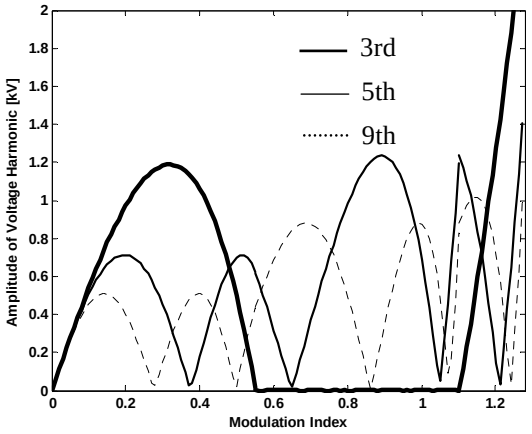


Fig. 6 Harmonic content of the output voltage

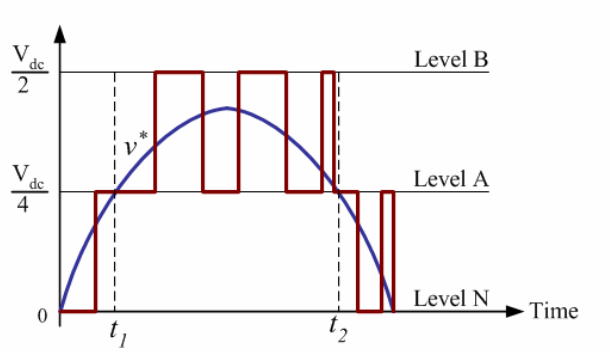


Fig. 7 Voltage Waveform of a 5-level NPC.

Fig. 5 illustrates these switching angle α_1 and α_2 and Fig. 6 depicts the amplitude of the first harmonics. Concerning the harmonic content this method seems to be the most suitable so far. With an increasing as well because this introduces new degree of freedom and more harmonics can be eliminated.

$$\alpha_1(m_a)=\begin{cases}\arccos\left(m_a\dfrac{\pi}{2}\right) & 0\le m_a\le\dfrac{\sqrt{3}}{\pi}\\ \arccos\left(\dfrac{m_a\pi}{4}+\dfrac{1}{12}\sqrt{36-3m_a^2\pi^2}\right) & \dfrac{\sqrt{3}}{\pi}\le m_a\le\dfrac{2\sqrt{3}}{\pi}\\ \arccos\left(m_a\dfrac{\pi}{4}\right) & \dfrac{2\sqrt{3}}{\pi}\le m_a\le\dfrac{4}{\pi}\end{cases} \quad (14)$$

$$\alpha_2(m_a)=\begin{cases}\dfrac{\pi}{2} & 0\le m_a\le\dfrac{\sqrt{3}}{\pi}\\ \arccos\left(\dfrac{m_a\pi}{4}+\dfrac{1}{12}\sqrt{36-3m_a^2\pi^2}\right) & \dfrac{\sqrt{3}}{\pi}\le m_a\le\dfrac{2\sqrt{3}}{\pi}\\ \arccos\left(m_a\dfrac{\pi}{4}\right) & \dfrac{2\sqrt{3}}{\pi}\le m_a\le\dfrac{4}{\pi}\end{cases} \quad (15)$$

Characteristic of DC-link Capacitors

In Fig.3, the equivalent circuit of a 5-level NPC inverter is depicted. The DC-link voltage is divided into four different capacitors, which all have the same capacitance and voltage. Due to the modulation of a sinusoidal output voltage the load will be connected to the upper three voltages (B, A, N) during the positive semi-cycle and to the lower voltages for the negative half-wave. For the subsequent analysis only the positive half-wave is used, therefore only the three switching states B, A and N have to be considered.

First, the voltage stability problem of a five-level diode-clamped converter will be briefly described. Fig. 7 shows one half period of the output voltage of the inverter. As long as the reference voltage (v^*) has a magnitude which is below the voltage of level A, the output is switched between the two potentials A and N. therefore, only the inner capacitor is discharged. If the reference voltage exceeds the value of Level A the modulation charges and the output is switched between the potentials A and B. It becomes obvious that the two capacitors are not discharges equally.

The reason for the different discharge is, that the inner capacitor is constantly discharged during the first semi-cycle whereas the outer one is only discharged between t_1 and t_2. Hence, the voltage distribution in the DC-link cannot be kept constant for active power transmission. Consequently, a five-level diode-clamped converter can only be used for active power transmission if a Back-to-Back solution is used.

Although it is not possible to achieve stable DC levels with a five-level diode-clamped converter for a standard drive application it could be possible to use this circuit for the short operation times of custom power devices. One solution could be a different size of the inner and the outer capacitor. The disadvantage of different capacitors is, that the DC-link cannot be recharge by one source. Hence, each capacitor has to be charged separately. Since the recharge must not be very fast for custom power devices, relatively small sources can be used and therefore this is no real disadvantage for such a system.

3. FIGURES AND TABLES SIZING OF CAPACITORS AND ENERGY

Ratio of Capacitances

The positive and negative half-waves lead to the same discharge of the two upper and two lower capacitors. As a result, the calculation effort can be reduced to one half cycle. The calculate the charge Q_1 drawn from each capacitor, the half cycle between 0 and T/2 is divided in two parts. During the first part, the output is only switched between the levels N and A (t = [0, t_1] & [t_2, T/2]). For the duration of the second interval (t = [t_1, t_2]) the voltage level is switched between the levels A and B. The first step is to calculate the borders of the interval, therefore t_1 and t_2 must be calculated. These times can be calculated by considering the fact that, as soon as the reference voltage elapses the voltage of level A, the second starts ($v^*(t) = V_m sin(\omega t) = V_{dc}/4$). Using these fact two equations can be derived.

$$t_1=\frac{T}{2\pi}\arcsin\left(\frac{V_{dc}}{4V_m}\right)=\frac{T}{2\pi}\cdot x \quad (16)$$

$$t_2=\frac{T}{2\pi}-t_1=\frac{T}{2\pi}\cdot(\pi-x) \quad (17)$$

where $x=\arcsin\left(\dfrac{V_{dc}}{4V_m}\right)$

Based on these two equations and by comparing the voltage-sec area of the reference voltage and the output voltage, the complete time interval during which the output voltage is connected to level A(t_A) and to level B(t_B) can be calculated. Within the first section, the inverter is switched between the neutral point and level A. By comparing the voltage-sec areas of the reference voltage and the output voltage the time t_{A1} can be calculated. This is the interval where the output is connected to level A, as long as the reference voltage is below the magnitude of level A. This leads to the following equations (18).

$$\frac{V_{dc}}{4}\cdot t_{A1}=\int_0^{t_1}V_m\sin(\omega_0\cdot t)\cdot dt+\int_{t_2}^{T/2}V_m\sin(\omega_0\cdot t)\cdot dt \quad (18)$$

$$t_{A1}=\frac{8\cdot V_m\cdot T}{2\cdot\pi\cdot V_{dc}}\cdot(1-\cos x)$$

Analog to these considerations the other needed time intervals can be calculated. In this case the voltage-sec area for the section where the reference voltage is above level A has to be considered. The time t_{A2} is equal to the interval during which level A is connected to the output and during t_B the output voltage is equal to level B. Thus, the equations (19) and (20) can be derived.

$$t_{A2}=T\cdot\left(1-\frac{2}{\pi}\cdot x-\frac{4\cdot V_m}{\pi\cdot V_{dc}}\cdot\cos x\right) \quad (19)$$

$$t_B=T\cdot\left(\frac{4\cdot V_m}{\pi\cdot V_{dc}}\cdot\cos x+\frac{x}{\pi}-\frac{1}{2}\right) \quad (20)$$

Finally, the time intervals for level A and B connected to the output can be derived. This leads to the total time t_A during which level A is connected to the output.

$$t_A = t_{A1} + t_{A2} = T \cdot \left[1 - \frac{2 \cdot x}{\pi} + \frac{4 \cdot V_m}{\pi \cdot V_{dc}} \cdot (1 - 2 \cdot \cos x) \right] \quad (21)$$

To determine the change drawn from the capacitors the load current must be assumed next. To get a worst case estimation a pure ohmic load is considered. Therefore, a constant current is drawn from each capacitor during the time intervals. Whereas during t_A charge is only drawn from the inner capacitor, during t_B both capacitors are discharged. Using the current (I_{LA}, I_{LB}) during the two time intervals the charge drawing from the capacitors can be derived, with Q_1 draw from the outer capacitor and Q_2 from the inner one.

$$Q_1 = \frac{V_{dc}}{2R} t_B \qquad \text{with } I_{LB} = \frac{V_{dc}}{2R} \quad (22)$$

$$Q_2 = \frac{V_{dc}}{2R} t_B + \frac{V_{dc}}{2R} t_A = \frac{V_{dc}}{2R} \left(t_B + \frac{t_A}{2} \right) \text{ with } I_{LA} = \frac{V_{dc}}{4R} \quad (23)$$

via the amplitude modulation index ($m=V_m/(V_{dc}/2)$) the needed quotient of the charges draw from the capacitors can be calculated with the following expression.

$$\begin{aligned} q &= \frac{Q_1}{Q_2} = 2\cos x + \frac{1}{2m}(2x - \pi) \\ &= 2\cos\left(\arcsin\left(\frac{1}{2m} \right) \right) + \frac{1}{2m} \left[2\left(\arcsin\left(\frac{1}{2m} \right) \right) - \pi \right] \end{aligned} \quad (24)$$

Since both capacitors will be charged to the same voltage, equation 13 expresses also the needed capacitor ratio for a constant discharge of the outer and the inner capacitor. It becomes obvious that this quotient depends on the modulation index, therefore it is not possible to achieve equal discharge for all modulation indexes. If the modulation index is below 0.5 the outer capacitance will not be discharged, because only the level A and N will be connected to the output.

In Fig. 8 the derived equation is depicted for a modulation index from 0.5 to 1.2. As expected, a low modulation index leads to a very large capacitor C_2, because for a modulation index below 0.5 the energy will only be drawn from the inner capacitor. Therefore, a low index leads to large discharge of the inner capacitor and a lower for the outer capacitor. On the contrary, a large modulation index corresponds to a long time interval in which the output is switched between level A and B. Consequently, both capacitors are discharged during most of the period and the needed ratio is approaching unity.

In view of the fact the custom power devices needs different modulation indexes – depending on the sag depth and the needed compensation time – it is also not possible to achieve an equal discharging. One advantage f a custom power devices is that the minimum modulation index is above 0.5, because shallow sags can be compensated up to the maximum voltage of 10% above the nominal value. Therefore, a higher modulation index can be chosen to assume a proper functionality of the custom power devices. As a consequence, an average value of the modulation index should be used to assure compensation with the five-level diode-clamped converter topology. In most custom power devices applications the amount of energy needed for the application can easily be calculated. Therefore, it is important to calculate the different capacitances from this value by considering the needed ratio derived in equation (24). The stored energy and the needed capacitors can be calculated with the following equation (25).

$$E_{dc} = 2 \cdot \frac{1}{2} \cdot (C_1 + C_2) \cdot \left(\frac{V_{dc}}{4} \right)^2 \quad (25)$$

$$C_1 = \frac{16 E_{dc}}{V_{dc}^2 \left(1 + \frac{1}{q} \right)} \qquad C_2 = \frac{16 E_{dc}}{V_{dc}^2 (1 + q)}$$

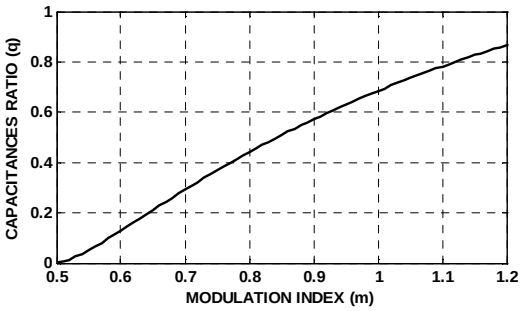


Fig. 8 Needed ratio of capacitances depending on modulation index

Reduced Amount of Energy Needed

The main advantage of different capacitance is the reduced amount of energy needed for the compensation process. In general, the minimum amount of energy is determined by the value needed for a successful compensation, therefore it can be calculated by considering the worst case failure and the minimum compensation time. If a standard design is chosen all capacitors will be equal, leading to a similar amount of energy within each capacitor.

Due to the unsymmetrical discharge of the capacitors a larger portion of energy is drawn from the inner capacitors. Consequently, these capacitors will be discharged quit fast and the semiconductors needed to block higher voltages. Hence, the amount of energy must be increased to avoid these problems. By varying the capacitances this oversizing can be reduced significantly, because the capacitors are designed according to the needed energy during compensation.

Considering the needed size of the inner capacitor (C_2) the needed amount of energy can be calculated. For the standard solution all capacitors will be design equally, whereas for the presented solution the outer capacitor will be reduced according to the calculated ratio (equation (26)).

$$E_{S\tan dard} = 4 \cdot \frac{1}{2} \cdot C_2 \cdot V_{dc}^2 = 2 \cdot C_2 \cdot V_{dc}^2 \quad (26)$$

$$E = 2 \cdot \frac{1}{2} \cdot C_2 \cdot V_{dc}^2 + q \cdot \frac{1}{2} \cdot C_2 \cdot V_{dc}^2$$

This leads to the following equation:

$$\frac{E}{E_{S\tan dard}} = \frac{1+q}{2} \quad (27)$$

It should be kept in mind that the ratio between the capacitors cannot be reduced too much, because the voltage of the outer capacitor is needed to assure a correct compensation of the load voltage and therefore the energy storage in these devices has to be sufficient. Various simulations were accomplished to find the minimal value for the capacitor ratio for worst case scenarios. In the presented application the lowest ratio realized was 0.4, leading to 30% less energy needed for the custom power devices application. As a consequence, the enormous cost for the large DC-link capacitors can be reduced considerably compared to a standard 5-level design.

4. SIMULATION RESULTS

To prove the calculation from the previous section, simulations were done with a DVR based on a five-level diode-clamped converter. Fig.9 shows the DC-link voltage during a three-phase sag under full load conditions. In this case, the remaining voltage is 75% of the nominal voltage with a total compensation power of 10 MW.

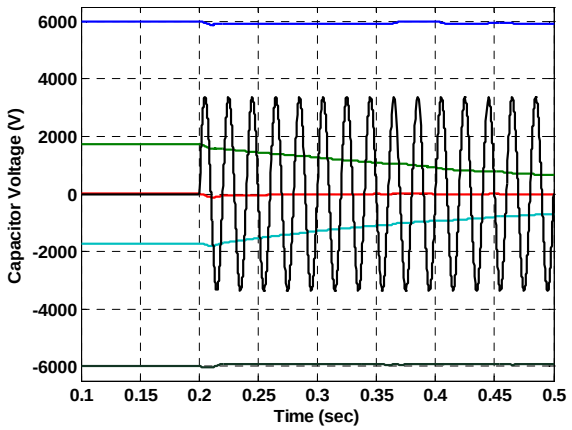


Fig.9 DC-link voltage during the compensation of a three-phase sag with ohmic load.

At approximately 200 ms, the sag is detected and the custom power devices starts to compensate the voltage. From that point on the DC-link constantly discharged. The ratio of the outer and the inner capacitor is 0.4, which corresponds to a modulation ratio of 0.75. It becomes obvious that the capacitors are not discharged equally, because the modulation ratio changes during the compensation. Due to the needed large energy storage device, a custom power devices is only used for short compensations of 300 ms under full load conditions [6]. During the 300 ms the voltage difference is still quite low, so that the inverter is still operational. Therefore, it was proven that the five-level diode-clamped converter can be used for an active power compensation with different capacitances. As already mentioned, the load was assumed to be ohmic to calculate the needed capacitor ratio for a worst-case scenario. This calculated ratio can also be used for different displacement factors, to prove this the same capacitors were used for a similar load and voltage sag. The power factor of 0.8. In Fig.10 the different DC-link voltages are depicted. By comparing these results to the previous pure ohmic load it becomes obvious that the voltage difference between the outer and the inner capacitors has decreased. Thus, the previously described assumption leads to a worst-case scenario and can be used for the design of a custom power devices based on a five-level diode-clamped converter topology.

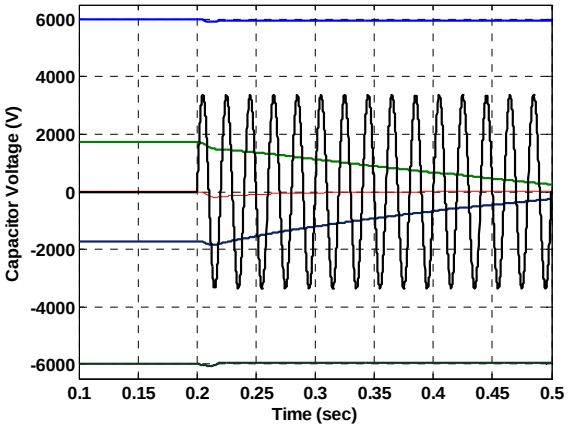


Fig.10 DC-link voltage during the compensation of a three-phase sag.

5. CONCLUSION

One major power quality problem in distribution grids are voltage sags, which lead to production losses in sensible processes. For medium voltage and high power loads custom power devices are one solution. Since the power of the protected loads is constantly increasing, new inverter concepts should be examined, i.e. higher number of levels. Therefore, a five-level diode-clamped converter was examined for this application. The main disadvantage of the five-level diode-clamped converter topology is that it can only be used in a back-to-back configuration if active power is needed. Otherwise, the capacitor voltages will deviate from each other and a steady-state operation is not possible. However, for custom power devices applications active power is needed, but only for a short time interval.

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