An Improved PWM Technique for Two-Level Quasi Switch Three-Phase Boost Converter

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ABSTRACT

This article presents a modified pulse-width modulation approach for the two-level quasi-switch three-phase power electronic inverter (3P2LqSBI) to extend the modulation indicator (m) and eliminate the ripple of the current in inductors. The offset function in the improved technique helps to increase the range of the modulation index. This increase shoot-through time in the inverter mode. The short-circuit pulses are inserted appropriately into zero vectors for the voltage boosting, and this is not to affect the output voltage. In theory, increase the short-circuit ratio on the inverter side will reduce the duty cycle in DC boost, thereby helping to reduce the ripple current in the input inductor. The simulation results and the analyses in the paper verify the effectiveness of the proposed technique.

1. INTRODUCTION

The use of voltage source inverters (VSI) is expanding in a variety of specialized systems, including transportation applications, uninterruptible power supply (UPS) systems, wind turbine power systems, and residential photovoltaic systems [1-3]. The conventional two-level inverters are regularly used as the buck converter. However, to use VSI for voltage boost purposes, a DC/DC boost converter is required to be added along with the DC/AC inverter. This leads to increasing the size and manufacturing costs of the inverters [4-5]. Furthermore, the VSI does not allow two-switches in a phase to be on together (Shoot Through-ST). This phenomenon short-circuits the input voltage source and causes damage to the system. A dead-time unit is often used to limit the effects of ST. However, using a dead-time unit degrades the converter performance.

Overcoming the above drawback, the Z Source inverter, shown in Fig. 1, which was introduced by F Z P in 2003 [6]. This structure is known as a power converter and is capable of buck-boost direction and well-controlled against short circuit of the leg inverter. However, the Z-source inverter still has some disadvantages, such as the discontinuous current at the input side and the high voltage stress on the capacitor.

In 2008, to limit the disadvantages of the Z-source inverter, J. Anderson and F. Z. Peng introduced the quasi Z-source inverter (qZSI), illustrated in Fig. 2. Then there are more publications related to [7]. Among them, the publication of M. K. Nguyen in 2015 is well known. These publications are all aimed at improving the circuits that can help to downside the passive components but still keep the advantages of the Z source, the quasi-switch boost inverter (Fig. 3), which is introduced in [8]. In the years of 2018 and 2019, there has been diverse research on voltage source inverters, such as T-shaped voltage source inverters, VSI of a switch self-correction ability [9,10].

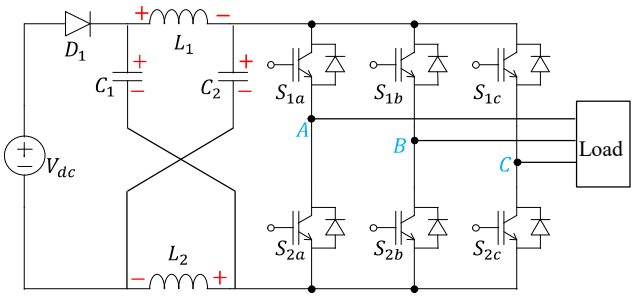

Fig. 1. Z-source inverter.

This paper presents a pulse width modulation using an improved carrier signal technique and an offset function to extend the modulation indicator on three-phase two-level qSBI (3P2LqSBI). The operation of the proposed algorithm in 3P2LqSBI was analyzed and verified by PSIM simulation. This article is structured as follows: the second part illustrates the qSBI modes analysis; the third part shows

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the analysis and recommendation of a PWM control technique for 3P2LqSBI; and part 4 presents simulation results and the proposed PWM technique. The article ends with conclusions and recommendations.

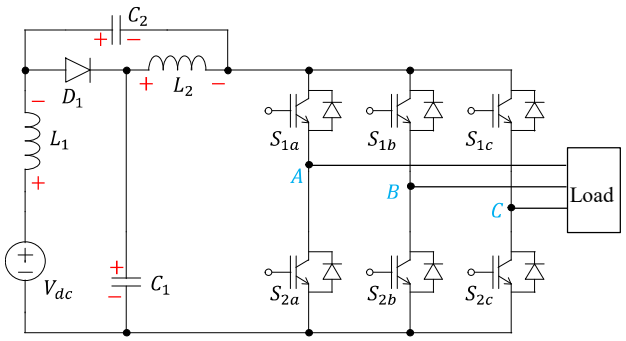


Fig. 2. Quasi Z-source inverter (qZSI).

2. STRUCTURE OF 3P2LQSBI

The three-phase two-level quasi switch boost (3P2L qSB) is combined by two main parts: the quasi Switch Boost (qSB) and the 3-phase two-level voltage source power electronic converter, as shown in Fig. 3.

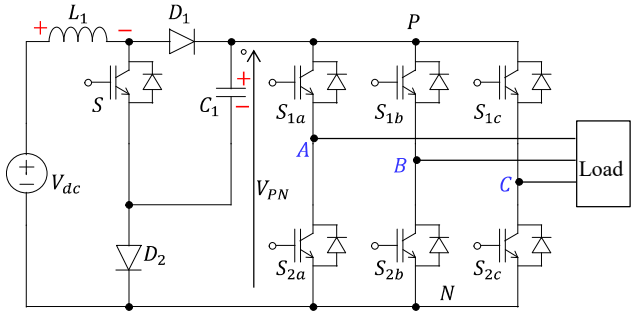


Fig. 3. 3P2LqSBI scheme.

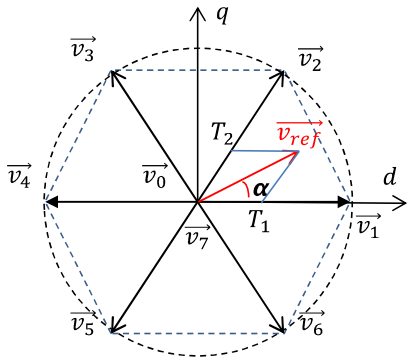


Fig. 4. 3P2LqSBI space vector.

The qSB network, which is analyzed in [8], [11], basically consists of one inductor (Li), one capacitor (C1) and dual diodes (D1, D2). Two outputs of the qSB network (P and N) will feed energy to the 2-level inverter in phases a, b, c, in which each phase consists of 2 IGBTs.

By switching on S_{1x} or S_{2x} (x = a, b, c), the output voltage on 3P2L qSBI is likely to be 0V or V_C. The phase voltages are generated by changing the state of eight switching vectors in vector space (Fig. 4). The desired voltage vector ($\vec{v_{ref}}$) shown in Fig. 4 can be obtained from the switching vectors $\vec{v_0}$, $\vec{v_1}$, $\vec{v_2}$, and $\vec{v_7}$ as follows:

$$\vec{v_{ref}} = T_0.\vec{v_0} + T_1.\vec{v_1} + T_2.\vec{v_2} + T_7.\vec{v_7} \quad (1)$$

where, vectors $\vec{v_0}$ and $\vec{v_7}$ are zero vectors, and T_0, T_1, T_2, and T_7 are the switching times alongside the switching vectors $\vec{v_0}$, $\vec{v_1}$, $\vec{v_2}$, and $\vec{v_7}$. In the f zero vector, S_{1x} switches are connect to P or S_{2x} switches are connect to N. Hence, the voltage V_{PN} does not relevant to the load, so it is practical to make a short circle P-N (shoot through) for energy accumulation in the inductor L_i. In other words, there are three main operation states of the 3P2L qSBI network: "No Shoot Through (NST)", " Shoot Through (ST)" and "Shoot Through on the boost side (SB)". Fig. 5 shows the operating states of 3P2L qSBI.

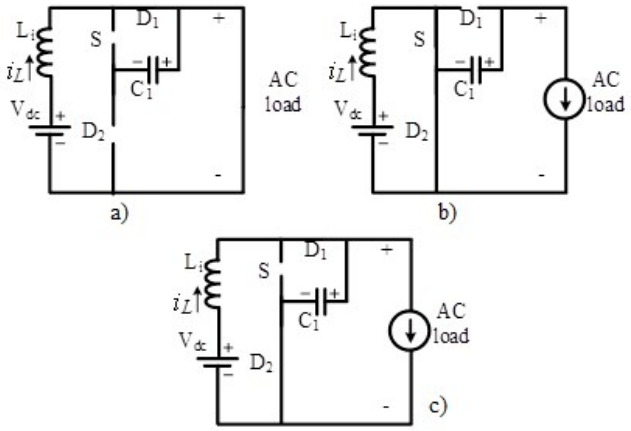


Fig. 5. Operating states of 3P2LqSBI.
a) ST state b) ST state on the boost side c) NST state

2.1. Principle of operation

The switching diagram which shown in Fig. 6 presents the operaring states of 3P2LqSBI in Fig. 5.

In Fig. 6, the voltages V_{carI} and V_{carS} are triangle carrier signals for the 3P2LVSI and for the switch S of the boost side, respectively. The triangle carrier signals (VcarI and VcarS) have peak to peak voltage as 1 and zero DC offset. Each carrier signal can have two possible short-circuit pulses in a periodical cycle, so there are four short-circuit pulses in case of using two separate carrier signals. In order to get those short-circuit pulses equidistant, the phase shift of two triangular carrier signals is $\frac{\pi}{2}$ rads. The voltages V_{STP} and V_{STN} are the control voltage for short circuit on the inverter side, while V_{SP} and V_{SN} are the control voltage for switch S on boosting side.

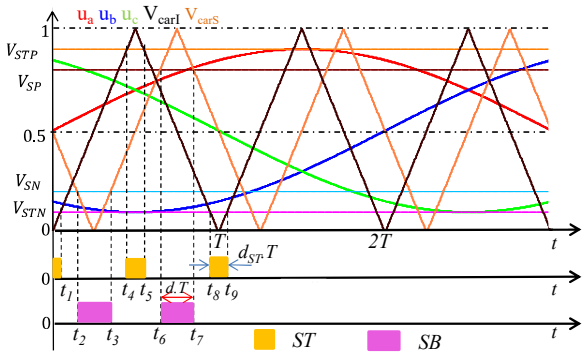


Fig. 6. Waveforms of switching diagram of the improved converter 3P2L qSBI.

2.1.1. Shoot Through (ST) state

During the ST state in the 3P2L VSI scheme, the switches S1X and S2X are turned on together as shown in Fig. 5 (a). At the edge time, the switch S is off, diode D1 is in the state of forward biased and diode D2 is reverse biased. The lifetime of this state in the period T of the carrier signal is (2dST.T) second, where dST is the duty cycle of the switches on the DC/AC side that is controlled by the modulation voltage VSTP, VSTN (the Shoot Through voltage on the P and N) and carrier signal VcarI as shown in Fig. 6. During this time, the inductor is actively energizing from the source Vdc and capacitor C1 is isolated from the circuit. The voltage stress on the inductor is determined as follows:

$$L\frac{di_L}{dt} = V_{dc} \tag{2}$$

2.1.2. Shoot Through on the boost side (SB)

The SB state is depicted in Fig. 5 (b). At this state, the switch S is on, diode D2 is biased forward and diode D1 is reverse biased, while the other switches of the 3P2L VSI are in the off states. At this time, the Li inductor is charged from the source Vdc, capacitor C1 discharges, then energizes through the load. The voltage stress on the inductor is also determined as (2).

The total lifetime of the state SB in a period T of the carrier signal is a second, where d is the duty cycle of S that is drived by the modulation voltage VSP, VSN and the VcarS carrier signal.

2.1.3. No-Shoot-Through (NST) state

In the NST state, the switch S is off, the diodes D1 and D2 are forward biased as shown in Fig. 5(c). Capacitor C1 is charged, inductor Li discharges, supplying the energy to the load. The voltage stress on the inductor is:

$$L_i\frac{di_L}{dt} = V_{dc} - V_{C1} \tag{3}$$

2.2. Analysis

The total charging time of the Li inductor is 2.(d+dST).T so the voltage across capacitor C1 in steady state is determined as follows:

$$V_C = \frac{V_{dc}}{1-2d-2d_{ST}} \tag{4}$$

where, d is the duty cycle of S, dST is the duty cycle of the switches on inverter side.

The output voltage of inverter is determined:

$$\widehat{v_x} = m\frac{V_{PN}}{2} = \frac{m}{2}.\frac{V_{dc}}{1-2d-2d_{ST}} \tag{5}$$

where, m is the modulation indicator (or index) on the inverter side of the 3P2LqSBI. Hence the modulation voltages for 3 phases are determined:

$$\begin{cases} u_a = \frac{1}{2}m\sin(\omega t) + \frac{1}{2} \\ u_b = \frac{1}{2}m\sin\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{2} \\ u_c = \frac{1}{2}m\sin\left(\omega t - \frac{4\pi}{3}\right) + \frac{1}{2} \end{cases} \tag{6}$$

From the diagram in Fig. 6, the constrains is defined as follows:

$$0 \le m \le 1 \tag{7}$$

and

$$d_{ST} = \frac{1}{2} - \frac{1}{2}m \tag{8}$$

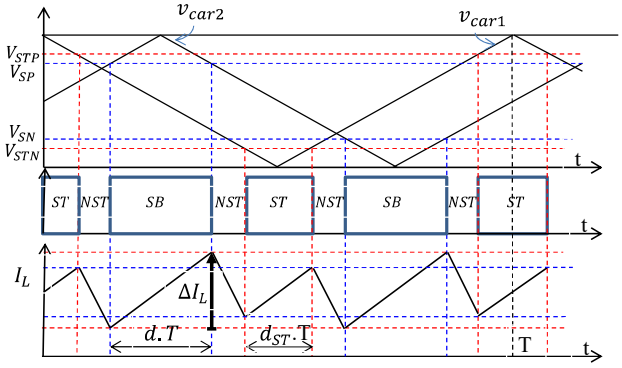


Fig. 7. Current waveform on L_i.

The inductor current ripple (ΔI_L) is therefore determined:

$$\Delta I_L = \frac{V_{dc}}{L_i}d.T \tag{9}$$

and ΔI_L is minimum when $d=d_{ST}$

From (9), it shows that if a Shoot Through state occurs (dST> 0), the modulation index m is always less than 1, and then it will result in a large voltage across the capacitor. It is

definitely the disadvantage of the current 3P2L qSBI control techniques. With the above analysis, the current flowing through the inductor Li has a waveform as shown in Fig. 7.

3. AN IMPROVED PWM METHOD FOR 3P2L QSBI

The condition (8) is rewritten as:

$$d_{ST} = 1 - \left(\frac{1}{2} + \frac{1}{2}m\right) = 1 - \hat{u} \tag{10}$$

where, $\hat{u}$ is the peak value of the 3-phase modulation voltage. On the other hand, in [12-15], it shows that adding an offset value to the modulation voltages ua, ub and uc did not affect the 3-phase output voltage of the circuit of the inverter (vx).

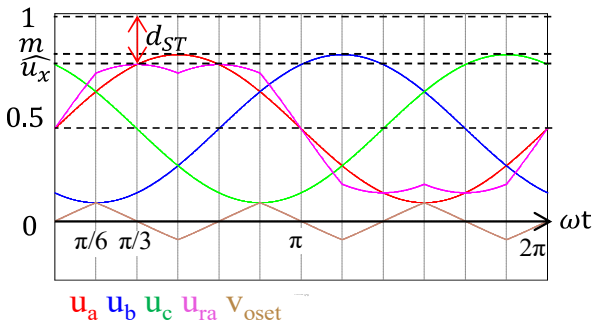


Fig. 8. Modulation voltage for 3P2L qSBI.

Hence, in the improved PWM carrier signal modulation technique, the authors propose an offset function, shown in (11).

$$v_{oset} = -\frac{\max(u_x) + \min(u_x)}{2} + 0{,}5 \tag{11}$$

Therefore, the modulation voltage for 3P2L VSI is

$$\begin{cases} u_{ra} = u_a + v_{oset} \\ u_{rb} = u_b + v_{oset} \\ u_{rc} = u_c + v_{oset} \end{cases} \tag{12}$$

Fig. 8 shows the offset-voltage (v_{oset}) (orange line), the initial 3-phase modulation voltage (u_a, u_b, u_c) and the phase-a modulation voltage within the offset (u_{ra}) (violet line), respectively. The peak voltage of the phase-a modulation voltage within the voltage offset is $\widehat{v_{ra}}$ that periodic of π/3 and is calculated:

$$\widehat{v_{ra}} = \frac{1}{2}m\sin\left(\frac{\pi}{3}\right) + \frac{1}{2} = \frac{m\sqrt{3}}{4} + \frac{1}{2} \tag{13}$$

From (13), the equation (10) is rewritten as:

$$d_{ST} = \frac{1}{2} - \frac{\sqrt{3}}{4}m \tag{14}$$

Combining (4) and (5), it can be seen that the duty cycle of S on DC/DC boost side, known as d, is according to the desired peak voltage ($\widehat{v_x}$) and the DC voltage (V_{dc}) input, which is determined as follows.

$$d = 0{,}5\left(1 - d_{ST} - \frac{V_{dc}}{2\widehat{v_x}}m\right) \tag{15}$$

The modulation voltages on the DC/DC boost and on the inverter are determined as:

$$V_{STN} = d_{ST},\ V_{STP} = 1 - d_{ST} \tag{16}$$

$$V_{SN} = d,\ V_{SP} = 1 - d \tag{17}$$

The condition for the duty cycle shoot through state is rewritten as:

$$d_{ST} = \frac{1}{2} - \frac{\sqrt{3}}{4}m > 0 \tag{18}$$

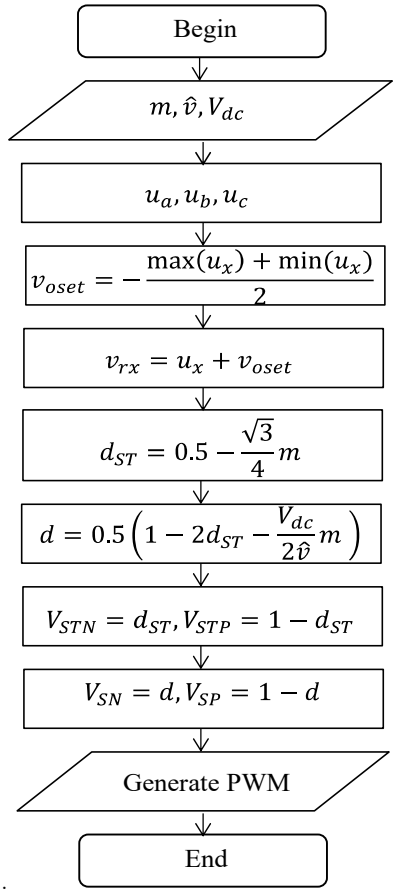


Fig. 9. The proposed PWM technique.

It means:

$$m < \frac{2}{\sqrt{3}} = 1{,}1547 \quad (19)$$

The proposed PWM technique is demonstrated in the flowchart shown in Fig. 9. The modulation indicator value m can increase by up to 1.1547, corresponding to an increase of 15.47% compared to the conventional PWM technique. Therefore, with the same desired AC voltage output and DC voltage input, the voltage across the capacitor can be reduced by 1.1547 times, compared to the conventional PWM techniques. Besides, with the same modulation indicator m and the same duty cycle d, the proposed method allows dST increase significantly compared to the other, thus obtaining the larger boost factor.If the same modulation index m and the same input and output voltage are used, then the total duty cycle (2d+2dST) is constant. So, increasing dST will lead to a decrease in d. Combining this analysis with the term in equation (10), it can be seen that the current ripples through the inductor decline rapidly. This is obviously the advantage of the new proposed technology compared to conventional PWM techniques.

4. SIMULATION RESULTS

The simulation is supported by PSIM software with the following sample set of parameters, which can be obtained by trial and error to achieve the optimal circuit requirement:

Table 1. Specification Data for Simulation

Specification of components		*Value*
Input voltage	V_{dc}	200 V
Output voltage	V_o	220Vrms
Carrier frequency	f_s	5 kHz
Inductance	L_i	3mH
Capacitance	C = C1	220 µF
LC Filter	L_f and C_f	3 mH and 10 µF
Resistive load	R_t	40 Ω

4.1. Effect of modulation index m

In this simulation, the desired AC voltage output is kept at 220Vrms as well as the DC voltage input is constant at 200V.

Fig. 10 illustrates the input current iL, DC/DC short-circuit pulse (SB-red line), inverter side (ST-blue line), DC-link voltage, and input voltage, voltage across capacitor C1. From Fig. (10), it can be seen that, in one triangle carrier signal cycle, the input current iL shows that Li is energized 2 times by switching on S, and 2 times charged when shoot through time on the inverter side, and 4-time discharges correspond to the 4 stages of transferring the energy to the AC load. The highest voltage DC-link is and the voltage across capacitor C1 is 542V.

The DC / DC boost ratio is $B_{DC} = \frac{V_{PN}}{V_{dc}}$ =2,71

When the modulation index m increases, the short-circuit time in the inverter side is reduced and will be zero when the modulation index m reaches m = 1.1547, as shown in Fig. 11. At this time, on the inductor, the input current iL has only 2-time charging processes and 2-time discharging processes, as in conventional DC/DC technology. It results the current ripples through the inductor is maximum. So, it is necessary to decrease m because when m is reduced, the duty cycle on the inverter side dST increases, the DC/DC boost duty cycle (d) decreases, and the ripple of the current through the inductor decreases (Fig. 12).

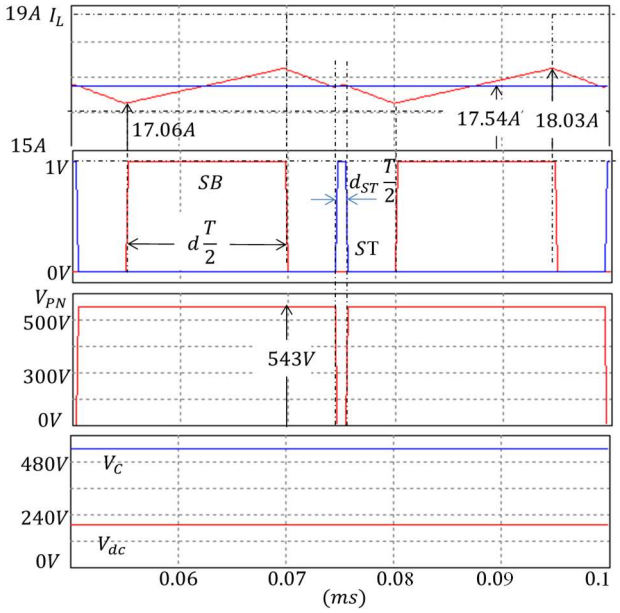


Fig. 10. Simulation results with V_{dc} = 200 V, V_o=220Vrms, modulation index m=1,1.

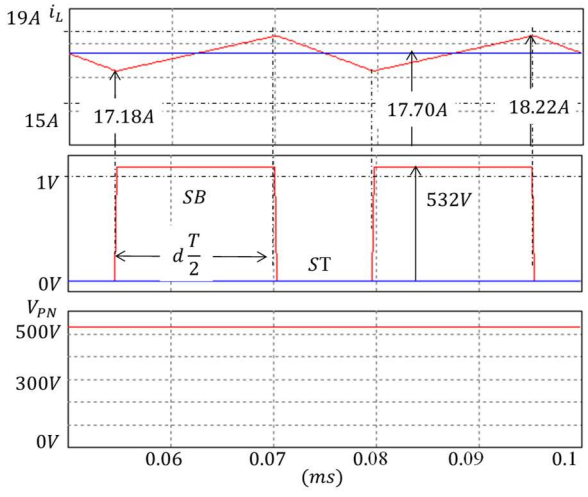


Fig. 11. Simulation results with V_{dc} = 200V, V_o= 220VRMS, modulation index m=1,1547.

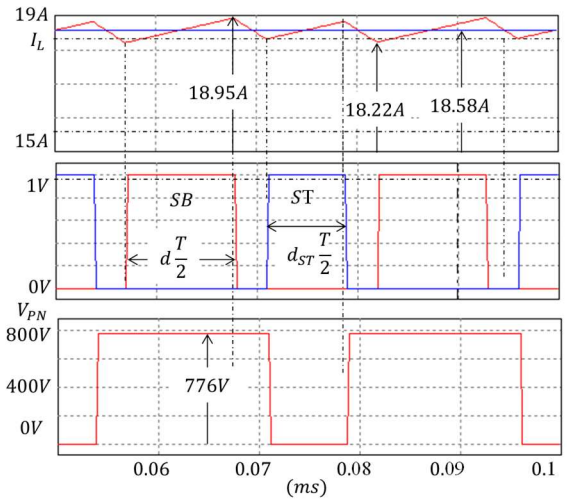
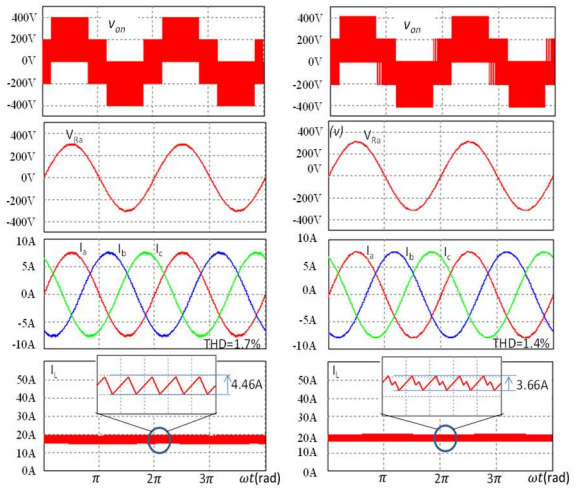


Fig. 12. Simulation results with V_{dc} = 200V, V_o=220Vrms, modulation index m=0,9.

When the shooting time on the inverter side is equal to the shooting time of SB, the ripple of the current through the inductor can be minimized, but there is a limit that the voltage across the capacitor will increase. Therefore, in the future, it is possible to propose a solution to optimize the ripple current through the inductor as well as the voltage across the capacitor.

4.2. Simulation results in comparison to conventional PWM technique with the same modulation index m

Fig. 13 shows the results of voltage stress on the capacitor and the current ripple by using traditional PWM technique and the proposed PWM on the 3P2L qSBI inverters with the same modulation index *m,* which consists of the load phase voltage (v_{AN}), voltage across load resistance (v_R), three-phase current, and current flows through the inductor L_i.



(a) (b)

Fig. 13. Simulation results for (a) traditional PWM and (b) proposed PWM technique with V_{dc} = 200 V, V_o =220Vrms, m=1.

The results from Fig. 13 shows that with the same voltage supply V_{dc} =200Vdc, the same voltage output 220Vrms and the same modulation index m, when applying the PWM technique, the current ripple through the L_i inductor decreases from 4,46A (in case of conventional PWM) down to 3,66A, equivalent to 17,9% (in case of proposed method). Besides that, because the ripple current is negligible, the V_{PN} voltage in the no shoot through circuit mode is almost imperceptible, so the total harmonic distortion (THD) of the current will also decrease from 1.7% to 1.4%. The simulation results are consistent with theoretical calculations in Table 2.

Table 2. Theoretical calculation in comparison to Conventional PWM technique with the same modulation index m

m	*PWM*	d_{ST}	*d*	V_C	ΔI_L
1	Traditional	0	0,339	622,25	4,46
	Proposed	0,067	0,272	622,25	3,66
0.9	Traditional	0,05	0,305	691,39	4,07
	Proposed	0,11	0,245	691,39	3,27
0.8	Traditional	0.1	0.271	777.82	3.62
	Proposed	0.154	0.218	777.82	2.90
0.7	Traditional	0.15	0.238	888.93	3.17
	Proposed	0.197	0.191	888.93	2.54

4.3. Simulation results in comparison to conventional PWM technique with the same ΔIL

In this simulation, in order to have the same current ripple, the DC sources will be the same in two cases and have a value of 200Vdc. The desired voltage on the AC voltage output is 220Vrms. Moreover, the duty cycle d on the DC/DC boost converter must be the same and satisfied:

$$d \geq d_{ST} \tag{20}$$

Leaning toward the above constrain, d values are selected to 0.3 and 0.25, respectively, therefore the modulation index *m* is determined:

- Case 1 traditional PWM

$$m = {(2\widehat{v_x}.2d)}\Big/{(2\widehat{v_x} - V_{dc})} \tag{21}$$

- Case 2 proposed PWM

$$m = {(2\widehat{v_x}.2d)}\Big/{(\widehat{v_x}\sqrt{3} - V_{dc})} \tag{22}$$

where, V_{dc} is the input DC voltage, 200Vdc; $\widehat{v_x}$ is the desired peak phase voltage. Thus, the simulation results will be

calculated as shown in Table 3. The simulation results for this case are shown in Fig. 14.

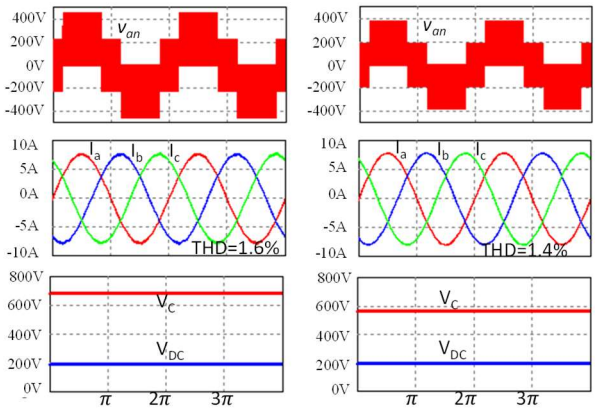


Fig. 14. Simulation results for (a) traditional PWM and (b) proposed PWM technique with V_{dc} = 200 V, V_o = 220Vrms, d=0.3.

Table 3. Theoretical calculation in comparison to conventional PWM technique with the same ΔI_L

D	*PWM*	*m*	d_{ST}	V_C *(V)*	ΔI_L*(A)*
0.3	Traditional	0,884	0,058	704	4
	Proposed	1,102	0,023	565	4
0.25	Traditional	0,737	0,132	845	3,3
	Proposed	0,918	0,102	678	3,3

The results from Fig. 14 shows that with the same data specification such as duty cycle on the DC/DC boost side, the power supply, and the AC voltage output, the load phase current, etc., the modulation index m in the proposed method is larger than in the traditional PWM technique. So the voltage stress on the capacitor is technically reduced from 704V to 565V.

A higher modulation index reduces total harmonic distortion (THD) by 1.4% when compared to the conventional PWM technique by 1.6%. The measured values in the simulation are once again consistent with the theoretical calculations.

5. CONCLUSION

This paper presented an improved PWM technique on the basis of conventional PWM technique for the 3P2L qSBI inverter. In this method, a voltage offset is added to the 3-phase modulation voltages and a function for determining the duty cycle d_{ST} of inverter are contributed. Besides the conventional Buck-Boost features, the proposed technique also has some advantages, such as being able to extend the modulation range up to 15.47%, which can reduce the voltage across capacitors, voltage across through the components, and the ripple of the input current.

Moreover, the simulation results have been analyzed and compared to the theoretical calculation, which showed the effectiveness and correctness of the proposed method.

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