A Transformer Less Continuous Input Current High Gain Boost Converter with Lower Voltage Stress and Minimum Component Count for PV Applications

Akkela Krishnaveni[1,2] and Rajender Boini[3,*]

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ABSTRACT

Photovoltaic system and other renewable power systems are increasingly using high DC gain Boost converters. The converter must have satisfactory dynamic and steady-state performance in addition to improved efficiency, is a pre-requirement for selecting in these applications. The DC voltage gain of a conventional boost converter (CBC) is restricted, and stress caused by the voltage across the switch is typically equal to the output voltage. In this study, a brand-new, reasonably duty-cycled, non-isolated high-DC voltage gain DC/DC converter design is presented by improving the quadratic boost converter (QBC). To drive the system and achieve the gain, just two no. of switches, two no. of switched inductors, two no. of capacitors, and two no. of diodes are used. Since it achieves a high voltage output at a lower duty cycle value, the duty cycle's operating range is wider. The converter also draws a constant input current while operating with greater efficiency at a reduced duty cycle. The dc/dc converter is ideal for photovoltaic applications because of its continuous input current, which is a desirable quality. A 200-watt, 24-volt prototype was examined, simulated in PSIM and a prototype was developed in laboratory created at a duty cycle of 0.62, a high DC-DC gain of 8.5 and 93% efficiency are attained. We compared the converter's number of components and semiconductor switches, voltage stress to that of other recently developed topologies and the proposed converter loss analysis also done. The results obtained from the experimental prototype have finally been used to validate the simulation. Theoretical and experimental analyses closely matched one another.

1. INTRODUCTION

New converter topologies for high-gain applications are needed as a result of the integration of renewable energy resources into Network infrastructure as well as the increased awareness of microgrids' importance in the economy and environment. It is primarily brought on due to the small amount of voltage that such sources produce, which has traditionally been the fundamental restriction on their employment. The use of active–passive inductor cells (APICs) is shown in an expandable converter [1].

Hard-switched, high-gain step-up DC-DC converters fall into two primary categories: isolated and non-isolated converters. Isolated converters that are used like flyback as well as forward converters, require a high-frequency transformer. As a result, increasing the transformer turns ratio can produce a higher gain. However, the associated magnetic component adds to the converter's size and weight. Additionally, voltage spikes are brought on by the transformer's leakage inductance [2]. To reduce the spike's amplitude and reuse the energy stored in the leakage inductance, active or passive clamp circuits are typically used. Costs and complexity are increased by these mitigations [3]. The proposed construction is based on series draining during switch-off periods and parallel charging of passive components during switch-on periods. Having reduced duty ratio spectrum, it is possible with the converter's high step-up voltage. The active switched inductors and passive switching capacitors are the foundation of the converter. Along with achieving high gain, the architecture additionally provides large efficiency, lowers voltage stress, and minimizes the circuit elements count [4]. Low voltage and current stress are provided by a family of transformer-less active switching inductors and switching capacitors in Cuk converters with high gain capability. To reduce conduction losses, semiconductors with reduced voltage ratings are utilized [5].

New high-gain boost converters with constant input current and SEPIC converters are suggested by the authors of [6]. Several methods have been developed to increase

[1]*Dept. of EEE, Chaitanya (Deemed to be University) Hanumakonda, Warangal, Telangana, India.*
[2]*Department of Technical Education, Government of Telangana, India.*
[3]*Dept. of EEE, Chaitanya (Deemed to be University) Hanumakonda, Warangal, Telangana, India.*
[*]*Corresponding author*: Email: rajender_eee@chaitanya.edu.in.

profit while decreasing costs and increasing efficiency. Switched-capacitor-based converter [7, 8] and switched capacitor/switched inductor-based converter [9–10] can produce large voltage gain with a short duty ratio and little voltage stress between the switching devices and these adapters are capable of employed in a broad variety of power levels. Still, they do possess several issues, including reverse recovery issues, larger losses, lesser efficiency, and issues with electromagnetic interference.

Transformer-less converters can be built using a variety of different theories, including i. voltage multipliers based on switching capacitors [11], ii. combinations of parallel-connected input and series-connected output circuits [12], iii. quadratic topologies [13], etc. The linked inductor's turn ratio is changed to get the correct gain, although doing so increases input current ripple. The coupled inductor topology issues were addressed by the high-gain converters suggested in [14–15]. There are two types of linked and non-coupled inductor converters for non-isolated DC-DC converters. It is frequently necessary to use a clamp circuit to recycle the stored energy and prevent ringing because coupled inductor converters have leakage inductance [16].

Coupled inductor converters thus share the same limitations as isolated converters discussed before [17–19]. High gain is produced by these converters at low duty ratios. A one switch high DC gain converter is advised to be used since it provides consistent input current and contains a limited quantity of active parts [20]. However, it has little power output and a lot of passive parts. A two-stage high DC voltage boost converter with one switch for usage in DC microgrid applications is displayed in [21]. This converter has the benefits of easy operation and low voltage stress across components. It still uses hard switching and has a sizable number of passive parts. In [22], a transformer-less converter built with coupled inductors and switching capacitor-boosting methods is introduced. These methods maximize voltage gain while using a low duty cycle. Despite the fact that the voltage pressures across the switches are lessened, it still operates with harsh switching, has a large number of elements, and huge losses, which results in a large size and high cost. In [23], a high-voltage gain switched-inductor doubled power switching DC/DC converter (SL-DS-DC) is presented.

A high-step-up DC/DC converter without a transformer is provided in [24] and consists of a switched-inductor with a quasi-Z source circuit. It is possible to obtain great efficiency and high voltage gain at low duty cycles. The key disadvantage is that when switched-capacitor cell density increases, semiconductor components also rise. In [25], a double boost-flyback converter was created. It combines two traditional boost-flyback converters with parallel input and floating output, increasing static gain while decreasing input current ripple. However, the input current would be discontinuous and have more ripple if the converter ran at a duty cycle lower than 0.5. Additionally, additional sensors are required due to the increased number of flyback cells, which makes the system bigger and more expensive.

The authors presented new high Dc gain converters utilizing a voltage multiplier cell (VMC) in [26–27]. Popular converters like boost, single-ended primary-inductor converter (SEPIC), and conventional quadratic boost (CQBC) can be used with VMC to maximize the gain. High charging current is an issue for a VMC using switching capacitors, which leads to significant power losses. Additionally, employing a VMC results in a higher component count and which increase the converter's cost and decrease its level of reliability.

Interleaved boost converters are a different family of converters. To raise the voltage, an interleaved converter requires many VMCs [28–30] at the output. The authors of [31] suggested an extensible switching inductor-based high-gain converter. The converter in [31] employed numerous inductors to produce high gain yet had continuous input current and decreased switch stress. In [32], a brand-new hybrid converter was put forth for DC microgrids. For solar PV applications, a modified SEPIC converter was put forth in [33].

Using voltage doublers & switching capacitors, the authors of [34–35] recommended a quasi-converter. With merely a voltage doubler and one switch, the inventors of [36] demonstrated a revolutionary QBC. Authors in [37–40] have suggested some additional, recently created high-gain converters. Despite the high gain of these converters, there are a lot of passive parts.

The converter suggested in this paper is primarily innovative in that it features a quadratic gain with 4 no. of passive components. Since coupled inductors are not employed to boost gain, leakage inductance-related issues are not present. A quadratic voltage gain with low voltage stress across switches, simple control and high efficiency are some of the converter's further benefits. In subsequent sections, the Structure and operation of the suggested converter is explained, in sections 3 and 4 Steady-state gain and Voltage Stress Across Switches and Passive Component Design are explained. Sections 5 and 6, Comparison among other alternative Converters and experimental results are explained, in sections 7 and 8, Efficiency Calculation and the conclusions are covered.

2. THEORICAL DESIGN AND FUNCTION OF THE SUGGESTED CONVERTER

Figure 1 show suggested converters structure. It has 2 number of power switches, two capacitors, two inductors, and two diodes. One gate driver control signal for both power switches, the control signal is the same. Two operating modes are available, depending on the control signal. Both the switch-on and switch-off modes of operation are meant by this. The ways of operation are explained as follows:

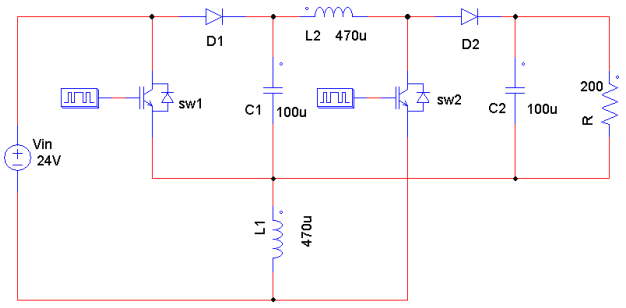

Fig. 1 Proposed Converter's organisational structure.

2.1 Switch-on mode of operation

In this operating mode, both switchers are switched ON at the same time. Because of this both diodes D1 and D2 have reverse bias. In Figure 2, the conduction diagram is displayed.in this mode of operation, the inductors both store the energy, Since the inductors & load get the electrical power from the capacitors as they discharge. As a result, the inductor current increases.

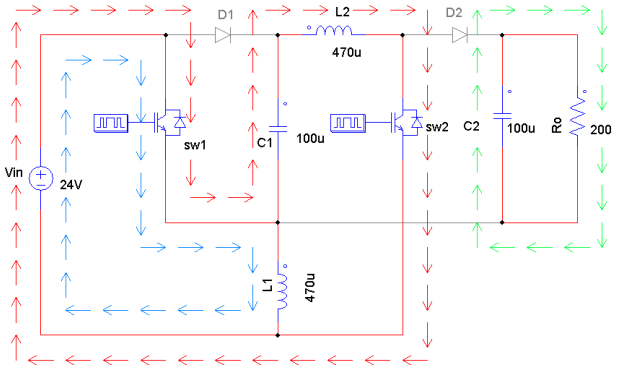

Fig. 2. Circuit Schematic for the Switch-On Mode of Operation.

For the switch on mode, the following governing equations apply:

$$V_{L1(ON)} = V_{IN} \quad (1)$$

$$V_{L2(ON)} = V_{IN} + V_{C1} \quad (2)$$

2.2 Switch-off mode of operation

Both the power switches are switched off in this mode and both diodes operate. During these modes of operation, both capacitors are charged, whereas the energy stored in two inductors is delivered to the load until current diminishes. In Figure 3, the conduction diagram is displayed.

The following is a list of the equations for this mode:

$$V_{L1(OFF)} = V_{IN} - V_{C1} \quad (3)$$

$$V_{L2(OFF)} = V_{C1} - V_{OUT} \quad (4)$$

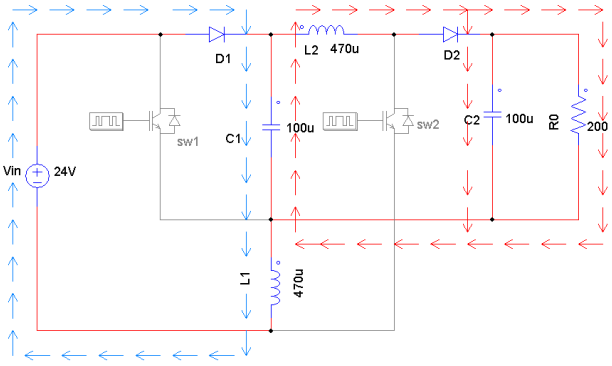

Fig. 3 Circuit Schematic for the Switch-Off Mode of Operation.

3. STEADY-STATE GAIN

The proposed converter continues to operate in CCM mode even under extreme load. Assuming that the suggested converter operates in CCM mode and that every component of the implementation is ideal.

Utilizing the volt-sec balance principle with inductor L_1

$$\int_0^{Ton} V_{L1(on)}(t)dt + \int_{Ton}^{T} V_{L1(off)}(t)dt = 0 \quad (5)$$

$$V_{in}.Dy.T + (V_{in} - V_{c1}).(1 - Dy)T = 0 \quad (6)$$

where, Dy is Duty cycle.

subtitute Dy = T_{on}/T in above equation, we get

$$V_{c1} = \frac{V_{in}}{(1 - Dy)} \quad (7)$$

Utilizing the volt-sec balance principle with inductor L_2

$$\int_0^{T} V_{L2}(t)\,dt = 0 \quad (8)$$

$$\int_0^{Ton} V_{L2(on)}(t)dt + \int_{Ton}^{T} V_{L2(off)}(t)dt = 0 \quad (9)$$

$$(V_{in} + V_{c1})Dy + V_{c1}(1 - Dy) = V_0(1 - Dy) \quad (10)$$

By substituting equation (7) in Equation (10) we get

$$V_{in}Dy + \frac{V_{in}Dy}{1-Dy} + V_{in}\left(\frac{1-Dy}{1-Dy}\right) = V_0(1 - Dy) \quad (11)$$

$$Voltage\ gain\ M = \frac{V_0}{V_{in}} = \frac{1 + Dy - Dy^2}{(1 - Dy)^2} \quad (12)$$

It is clear from Equation (12), then, that the proposed co nverter's voltage gain is quadratic.

4. PASSIVE COMPONENT DESIGN AND VOLTAGE STRESS ACROSS SWITCHES

Passive components are designed as follows, in 4.1 explained designing of inductors and in 4.3 designing of

capacitors

4.1 Design of inductors

Equation (1) is rewritten in differential form, we get

$$\Delta I_{L1} = \frac{V_{in} \cdot Dy \cdot T}{L_1} \quad (13)$$

Equation (2) is rewritten in differential form, we get

$$\Delta I_{L2} = \frac{(V_{in} + V_{c1})\, Dy \cdot T}{L_2} \quad (14)$$

By substituting equation (7) in Equation (14) we get

$$\Delta I_{L2} = \frac{(V_{in}(1 - Dy) + V_{in}) \cdot Dy \cdot T}{L_2 \cdot (1 - Dy)} \quad (15)$$

$$\Delta I_{L2} = \frac{V_{in}\,(2 - Dy) \cdot Dy \cdot T}{L_2 \cdot (1 - Dy)} \quad (16)$$

The average current through inductors L_1 and L_2 is:

$$I_{L1} = \frac{V_0}{R(1 - Dy)^2}\ ,\quad I_{L2} = \frac{V_0}{R(1 - Dy)} \quad (17)$$

The inductor L_1's minimal current flow as

$$(I_{L1})_{min} = \frac{V_0}{R(1 - Dy)^2} - \frac{V_{in} \cdot Dy \cdot T}{L_1} \quad (18)$$

For critical conduction mode $(I_{L1})_{min} = 0$
From equation (18)

$$\frac{V_0}{R(1 - Dy)^2} = \frac{V_{in} \cdot Dy \cdot T}{L_1} \quad (19)$$

$$L_1 = \frac{V_{in} \cdot Dy \cdot T \cdot R(1 - Dy)^2}{V_0} \quad (20)$$

Substituting V_{in} from equation (12) in equation (20)

$$L_1 = \frac{(1 - Dy)^2 . Dy \cdot T \cdot R \cdot (1 - Dy)^2}{(1 + Dy - Dy^2)} \quad (21)$$

$$L_1 = \frac{R . Dy . (1 - Dy)^4}{(1 + Dy - Dy^2) . f_s} \quad (22)$$

where, f_s is switching frequency =1/T

The minimum inductance necessary for the continuous conduction mode of operation

$$L_1 \geq \frac{Dy\ \cdot (1 - Dy)^4 \cdot R}{V_0 \cdot (1 + Dy - Dy^2) \cdot f_s} \quad (23)$$

The inductor L_2's minimal current flow as

$$(I_{L2})_{min} = \frac{V_0}{R(1 - Dy)} - \frac{V_{in}(2 - Dy) . Dy . T}{L_2(1 - Dy)} \quad (24)$$

For critical conduction mode $(I_{L2})_{min} = 0$
From equation (24)

$$\frac{V_0}{R(1 - Dy)} = \frac{V_{in}(2 - Dy) . Dy . T}{(1 - Dy) \cdot L_2} \quad (25)$$

$$L_2 = \frac{V_{in}(2 - Dy) . Dy . T . R}{V_0} \quad (26)$$

Substituting V_{in} from equation (12) in equation (26)

$$L_2 = \frac{(2 - Dy) . Dy \cdot (1 - Dy)^2 \cdot R}{(1 + Dy - Dy^2) \cdot f_s} \quad (27)$$

The minimum inductance necessary for the continuous conduction mode of operation

$$L_2 \geq \frac{(2 - Dy) . Dy \cdot (1 - Dy)^2 R}{(1 + Dy - Dy^2) f_s} \quad (28)$$

4.2 Design of capacitors

The lowest voltage ripple that is permitted across the capacitor must be considered while choosing a capacitor. The capacitor has stored the charge in on period as:

$$\Delta Q = C \Delta V_C \quad (29)$$

$$(I_{c1})_{on}\ \cdot T_{on}\ = C_1 \Delta V_{C1} \quad (30)$$

$$(I_{c1})_{on} = \frac{C_1 \Delta V_{C1}}{Dy \cdot T} \quad (31)$$

$$(I_{c2})_{on} = \frac{C_2 \Delta V_{C2}}{Dy \cdot T} \quad (32)$$

The current flowing through each capacitor when the switch is ON is as follows:

$$(I_{c1})_{on} = \frac{V_0}{R \cdot (1 - Dy)} \quad (33)$$

$$(I_{c2})_{on} = \frac{V_0}{R} \quad (34)$$

Equating equation (31) and (33), we get

$$C_1 = \frac{V_0\ . Dy . T}{R \cdot (1 - Dy) \cdot \Delta V_{C1}} \quad (35)$$

From equation (12) substitute V_0 value in equation (35), we get

$$C_1 = \frac{V_{in}(1 + Dy - Dy^2) . Dy}{R(1 - Dy)^3 \Delta V_{C1}\ \cdot f_s} \quad (36)$$

From equation (7) substitute ΔV_{C1}in equation (36), we get

$$C_1 = \frac{(1 + Dy - Dy^2) . Dy}{R(1 - Dy)^2 \cdot f_s} \quad (37)$$

Similarly Equating equation (32) and (34) and substituting equation (7) and (12), we get

$$C_2 = \frac{(1 + Dy - Dy^2) \cdot Dy}{R(1 - Dy) \cdot f_s} \quad (38)$$

4.3 Voltage stresses across switches S_{W1} AND S_{W2}

The voltage stress over the switches was calculated by equations (39) and (40)

$$V_{sw1} = \frac{V_{in}}{1-Dy} = \frac{V_0 \cdot (1-Dy)}{(1+Dy-Dy^2)} \quad (39)$$

$$V_{sw2} = \frac{V_{in}}{(1-Dy)^2} = \frac{V_0}{(1+Dy-Dy^2)} \quad (40)$$

The equations (39) and (40) show that the stress across the switches $_{Sw1}$ and S_{w2} is less than V_0.

5. COMPARISON AND EVALUATION OF ALTERNATIVE CONVERTERS

The high DC voltage gain converters addressed in the paper are contrasted in this section. Table 1 presents the comparison among similar recently proposed converters. Four inductors, six capacitors, and three diodes made up a modified buck-boost topology presented in [41], However, the large benefit could only be maintained by keeping the duty ratios high. The converter provided here produces a gain of even greater than thirty at this lower duty, whereas the converter recommended in [41] need to be operated at 0.8 duty to provide a gain of 15

Table 1. Analysis of component counts and voltage improvements across various topologies

Topology	Number of Switches and Diodes	Number of Inductors and Capacitors	Total Number of Components	Voltage Gain $(\frac{V_0}{V_{in}})$	Normalized Voltage Stress $(\frac{V_{sw}}{V_{in}})$
[41]	1+3	4+6	14	$\frac{3}{(1-Dy)}$	$\frac{1}{(1-Dy)}$
[42]	1+3	1+3	8	$\frac{2}{(1-Dy)}$	$\frac{1}{(1-Dy)}$
[43]	1+3	2+2	8	$\frac{Dy(2-Dy)}{(1-Dy)^2}$	$\frac{2}{(1-Dy)}$
[44]	1+5	3+7	16	$\frac{2+2Dy}{1-Dy}$	$\frac{1}{(1-Dy)}$
[45]	1+3	3+3	10	$\frac{Dy}{(1-Dy)^2}$	$\frac{Dy}{(1-Dy)^2}$
Proposed converter	2+2	2+2	8	$\frac{1+Dy-Dy^2}{(1-Dy)^2}$	$\frac{1}{(1-Dy)}$ $\frac{1}{(1-Dy)^2}$

The converter described in [42] featured one switch, three capacitors(C) one inductor (L) and three diodes, however it had a lower gain than the current converter. Common ground was a benefit of the quadratic buck-boost converter suggested in [43], It was improper since the gain was insufficient and the input current was irregular. Compared to the converter presented in [44], which includes 3 no. of inductors, 7 no. of capacitors, 5 no. of diodes and a single switch, it also has a lower voltage gain. The converter proposed in [45] also a quadratic converter Despite having three inductors and three capacitors, the converter suggested in [45] had a low gain and considerable switch stress.

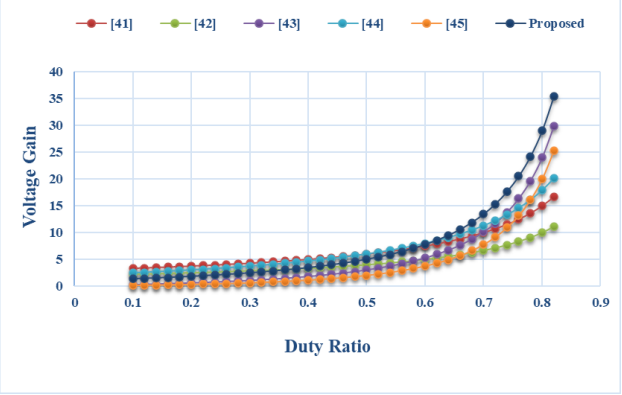

Fig. 4. Voltage gain comparison between various converters.

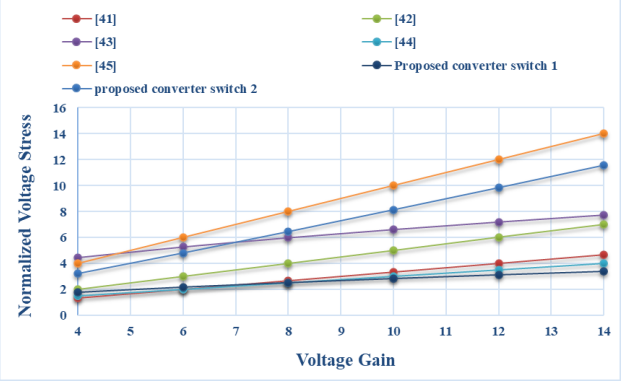

Fig. 5. normalized voltage stresses vs voltage gain graph of various converters.

Figure 4 shows that our suggested high-gain structure has an 8 times greater gain than the conventional boos converter at Dy = 0.6. Gain quickly rises from 0.7 Dy to 0.8 Dy. Due to the converter's lower parasitic resistance and lower losses in the ON state, in addition to its higher gain, it only uses 8 components. Figure 5 displays the switch of the converter under a normalised voltage stress. It is clear that the voltage stresses across the two switches in the converter varied. Compared to other structures, the tension across the switch Sw1 is the lowest. Although it was higher than Sw1, the stress across switch Sw2 was lower than VO. Additionally, it can be shown that the tension across Sw2 was lower than it was for the converters suggested in [45].

6. EFFICIENCY CALCULATION

The power loss in the various converter components is computed in this section. The converter's power loss is caused by the Resistance of switch in the ON state and diodes as well as parasitic resistances of passive components.

6.1 Power loss in inductors

The RMS and average currents flowing through an inductor can be taken as being equal if the current's ripple is ignored. The power loss caused by the parasitic resistance of inductors is illustrated in (41 and 42):

$$P_{L1} = \frac{{V_o}^2.r_{L1}}{R^2(1-Dy)^2} \quad (41)$$

$$P_{L2} = \frac{{V_o}^2.(2Dy-Dy^2)^4.r_{L2}}{R^2(1-Dy)^4} \quad (42)$$

where, r_{L1}& r_{L2} are the inductors' parasitic resistances.

6.2 Power loss in capacitors

Similar to this, the loss in capacitors caused by ESR is as follows:

$$P_{C1} = {I_{C1_{rms}}}^2.r_{C1} \quad (43)$$

$$P_{C1} = \frac{{V_o}^2.Dy.r_{C1}}{R^2(1-Dy)^3} \quad (44)$$

$$P_{C2} = {I_{C2_{rms}}}^2.r_{C2} \quad (45)$$

$$P_{C2} = \frac{{V_o}^2.Dy.r_{C2}}{R^2(1-Dy)} \quad (46)$$

6.3 Power loss in diodes

Knowing the RMS current allows one to determine the average current. the According to each diode's cumulative power loss:

$$P_{D1} = V_{D1}.I_{D1_{avg}} + {I_{D1_{rms}}}^2.r_{D1} \quad (47)$$

$$P_{D1} = \frac{V_{D1}.V_0}{R.(1-Dy)} + \frac{{V_o}^2.r_{D1}}{R^2(1-Dy)^4} \quad (48)$$

$$P_{D2} = V_{D2}.I_{D2_{avg}} + {I_{D2_{rms}}}^2.r_{D2} \quad (49)$$

$$P_{D2} = \frac{V_{D2}.V_0}{R.(1-Dy)} + \frac{{V_o}^2.r_{D2}}{R^2(1-Dy)} \quad (50)$$

where, V_{D1} *and* V_{D2} are the voltage drops across the diodes D_1 and D_2.

6.4 Power loss in the switch

Conduction loss $P_{sw_{cond}}$ and switching loss P_{sw} are the two different categories of switch losses. Following is a formula for calculating these losses:

$$P_{sw} = P_{sw_{cond}} + P_{sw_{ON}} + P_{sw_{OFF}} \quad (51)$$

$$P_{sw_{cond}} = {I_{sw_{rms}}}^2.r_{\,sw_{ON}} \quad (52)$$

where, $r_{\,sw_{ON}}$ is the MOSFET's ON-state resistance.

$$P_{sw1_{cond}} = \frac{{V_o}^2.(2Dy-Dy^2)^2.r_{sw1_{ON}}}{R^2.Dy.(1-Dy)^4} \quad (53)$$

$$P_{sw2_{cond}} = \frac{{V_o}^2.r_{sw2_{ON}}}{R^2.(1-Dy)^2} \quad (54)$$

$$P_{sw1_{ON}} = \frac{V_0.(2Dy-Dy^2).V_{in}.T_{ON}.f_s}{2R(1-Dy)^3} \quad (55)$$

$$P_{sw2_{ON}} = \frac{V_0.V_{in}.T_{ON}.f_s}{2R(1-Dy)^3} \quad (56)$$

$$P_{sw1_{ON}} = \frac{V_0.(2Dy-Dy^2).V_{in}.T_{OFF}.f_s}{2R(1-Dy)^3} \quad (57)$$

$$P_{sw2_{OFF}} = \frac{V_0.V_{in}.T_{OFF}.f_s}{2R(1-Dy)^3} \quad (58)$$

where, f_s is switching frequency, T_{ON} *and* T_{OFF} are turn on time and turn off time respectively.

Figure 6 shows the efficiency of the converter shown at various input voltage values. poor input voltages seem to result in a poor maximum efficiency. This is because higher converter losses resulted from the circuit needing a high current to provide the same amount of output power. The converter efficiency was outstanding if the input voltages were between 20 and 40 V. The output of a solar PV module is typically 24 V. Therefore, the suggested converter can be used to step up the voltage with great efficiency in the 150–250W power range.

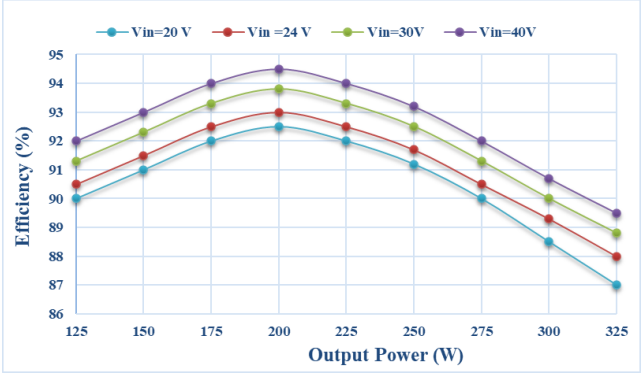

Fig. 6. Effectiveness of the converter at various input voltages.

7. SIMULATION AND EXPERIMENTAL RESULTS

Table 2 displays the converter's specifications. Figure 7(a) shows the PSIM simulation circuit of the proposed converter. Its outcomes are verified by creating a prototype in a lab. it is shown in figure 7(b) which is designed for 200 Watts power. In PSIM and laboratory prototype It is operated at a duty cycle of 0.62. According to Figure 8(a)

the output voltage V_O was 204 V which is close to the theoretical value. With resistive load of 200 Ω duty cycle 0.62 it is taking a current of 1.024 Amps which was show in figure 8(b). its corresponding input voltage and currents are show in figure 8(c) & 8(d). the converters average input current was around 8.2 Amps. From input current waveforms it is observed the input current is continuous. The key benefit of the converter was that the input current was continuous for heavy loads also. Figures 8 (e) shows the inductors current wave forms. Inductor one has the average value of 7 Amps while inductor two current was 3 Amps. Figure 8(f) is the FFT analysis of output voltage. It has only a fundamental value.

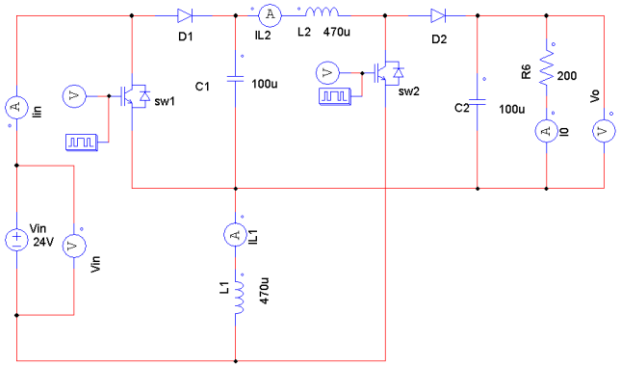

Fig. 7(a). PSIM Simulation circuit of suggested Converter.

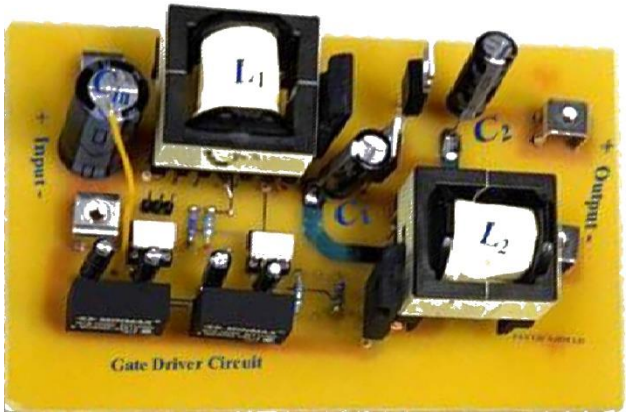

Fig. 7(b). Hardware prototype of proposed Converter.

Building a 200 W prototype, as shown in Figure 7(b), al lowed for testing of the converter's functionality. At a duty ratio of 0.62, the prototype was used. The output voltage V_O in Figure 9(a) was approximately equivalent to the theoretical value of 205V. As can be seen from the input current waveforms in Figure 9(b), the converter was in continuous conduction mode. Average input and output currents were discovered to be 8.5 A and 1.024 A respectively.

Table 2. Ratings of converter components

Components	Ratings
Input Voltage V_{in}	24V
R load	200 Ω
Switching frequency f_s	25KHz
Inductors	L1 = L2 = 470 µH, ESR = 0.2 Ω
Capacitors	C1 = C2 = 100 µF 200 V, ESR = 0.15 Ω
Ds1, Ds2 and Ds2	SF8L60USM
Gate Drivers IC	TLP250H

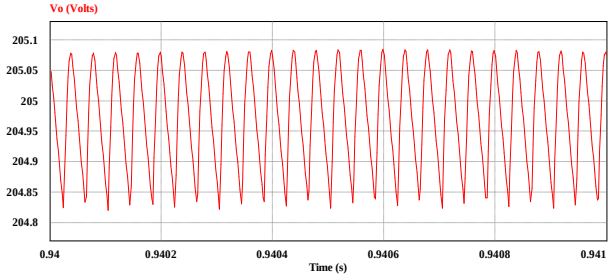

Fig. 8(a). Output voltage at a duty cycle of 0.62.

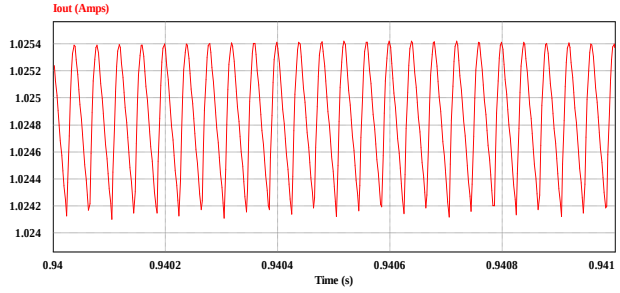

Fig. 8(b). output current at a duty cycle of 0.62

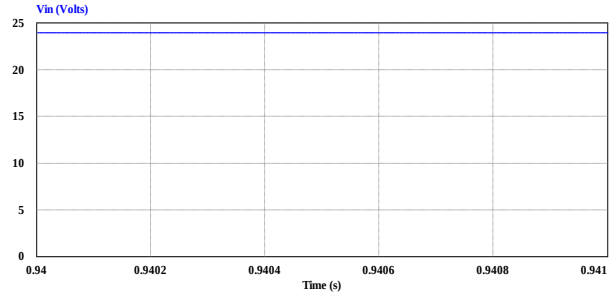

Fig. 8(c). Input voltage at a duty cycle of 0.62.

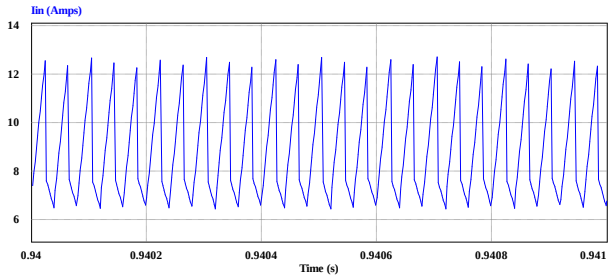

Fig. 8(d). Input current at a duty cycle of 0.62.

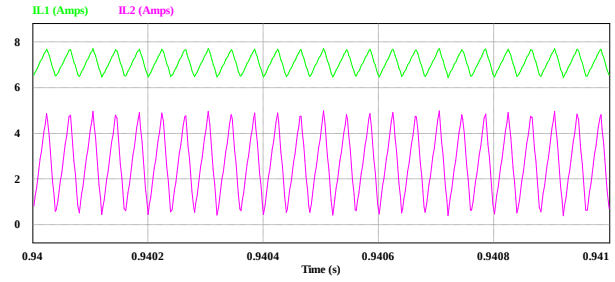

Fig. 8(e). Inductors current wave forms at a duty cycle of 0.62.

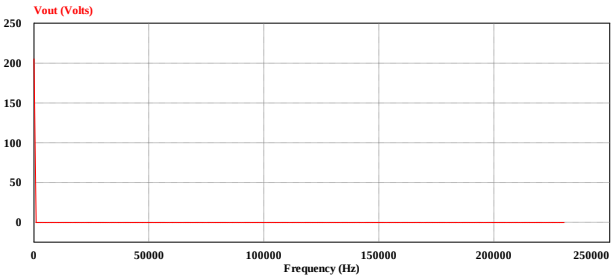

Fig. 8(f). FFT analysis of output voltage.

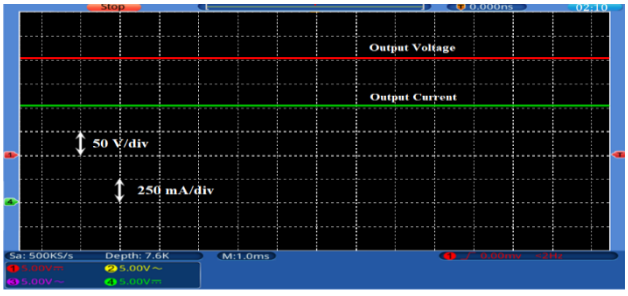

Fig. 9(a) & 9(b). Experimental output waveforms at duty cycle of 0.62.

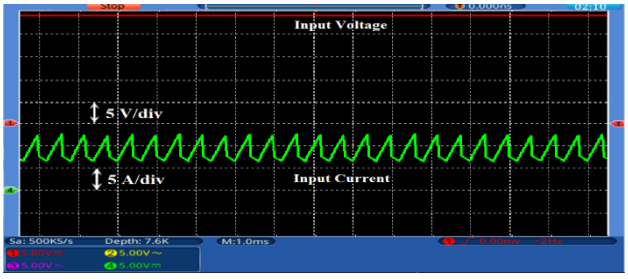

Fig. 9(c) & 9(d). Experimental waveforms of input voltage and input current at duty cycle of 0.62.

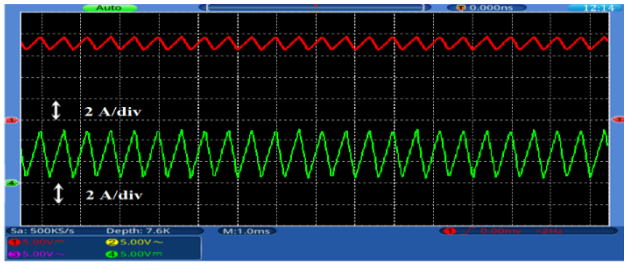

Fig. 9(e). Experimental waveforms of inductors current.

8. CONCLUSIONS

Analyses and a new high-gain converter were suggested. The proposed converter only needed a total of 8 no. of components to achieve significant voltage gain. Quadratic voltage gain converters typically are using more than 3 inductors and a number of diodes. switch and diodes are under low voltage stress as a result, a switch with a low voltage rating can be used, increasing efficiency and decreasing cost. For the converter, a 200W physical prototype has been created in order to actually test the study. As a result, the suggested converter is appropriate for medium power ranges up to 300W. The converter's primary attribute that extends the lifespan of solar PV panels is that it provides a continuous input current. Due to the converter's advantages, it can be used in solar PV, electric vehicles, fuel cells, and automobile applications.

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