Full Range Neutral-Point Voltage Balancing for Four-Level π-Type Inverter Using Carrier-Overlapped PWM

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ABSTRACT

Four-level π-type inverters face a major issue with neutral-point voltage imbalance, which prevents their widespread industrial application. This paper proposes a solution to this issue using carrier-overlapped pulse width technique. Three DC-link capacitors can be maintained at the rated value under ideal operating scenarios. However, to address voltage deviations caused by nonideal factors, the middle DC-link capacitor voltage is balanced by adjusting the duty cycles of switching signals, while the upper and lower DC-link capacitor voltages are balanced using zero-sequence voltage injection. Finally, to validate the feasibility of the modulation technique and voltage controllers, simulation results from the 3 kVA inverter prototype have been incorporated.

1. INTRODUCTION

In applications requiring high power and medium voltage (3–33 kV), multilevel inverters (MLIs) are an attractive solution due to their significant benefits over two-level inverters [1-3]. Recently, MLIs have become more appealing to researchers in low power applications due to their ability to improve power quality and power density, lower EMI, and provide a wide range of DC link voltages [4-6]. Several conventional MLIs, including the cascaded H-bridge (CHB) inverter, the neutral-point clamped (NPC) inverter, the flying capacitor (FC) inverter, and the modular multilevel inverter (MMC), have been successfully implemented in industry [5-7]. However, more power semiconductors and passive components are needed for MLIs with higher voltage levels, such as four or five levels, which increases the complexity of the circuit and control (modulation, capacitor voltage balancing, etc.).

In [8], a four-level π-type inverter was introduced, offering significant advantages, including reduced complexity and fewer components compared to other multilevel inverters. It eliminates the need for clamping diodes or flying capacitors and uses only six switching devices per phase leg, leading to simpler circuitry and lower total conduction losses. These features make it particularly suitable for high-density, low-voltage applications like electric vehicle systems and aircraft applications. Nevertheless, a major issue with the four-level π-type inverter is the capacitor voltage imbalance caused by having multiple clamping points in the DC-link, similar to the NPC circuit [8], [9].

In [10], the DC-link capacitor voltages can be balanced under certain operating conditions by injecting zero-sequence voltage (ZSV) into the reference voltages. For space-vector modulation (SVM), voltage balance cannot be achieved for the capacitor voltages under specific operating situations that exceed the theoretical boundary when using the nearest-three-vectors (NTV) technique[11]. Hardware solutions can overcome theoretical restrictions and improve the ability to balance capacitor voltages by configuring two converters to be coupled back-to-back [12], [13] or by using auxiliary balancing circuit [14], [15]. Nevertheless, these techniques require additional hardware, which increases the cost and complexity of the system.

To maintain capacitor voltage balance across all operating regions without the need for additional circuits, the carrier-overlapped pulse width modulation (COPWM) method, originally developed for NPC prototypes [16], [17], is applied to the 4L π-type inverter. COPWM is a novel modulation technique that overlays multiple carrier signals to generate more voltage levels in a sampling period. This scheme offers greater flexibility in achieving various control objectives, such as maintaining capacitor voltage balance.

Under this modulation method, the DC-link capacitors naturally achieve voltage balance under ideal conditions. However, to mitigate voltage deviations caused by non-ideal factors, a capacitor voltage control strategy should be developed. This is achieved through ZSV injection technique, which balances the voltage of the outer DC-link capacitors, and by modifying the duty ratios of switches to regulate the voltage of the middle DC-link capacitor. Simulation studies have validated the effectiveness of the

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COPWM method in the 4L π-type inverter under various operating conditions.

The proposed COPWM scheme for the 4L π-type inverter offers the following advantages:

- Maintains balanced capacitor voltages regardless of modulation index or load power factor.
- Eliminates the need for auxiliary balancing circuits.
- Enables easy implementation on any microcontroller, as COPWM is based on a level-shifted PWM scheme.

2. PWM MODULATION AND DC-LINK CAPACITOR VOLTAGE BALANCING CONTROL

2.1. Circuit configuration and switching states

The configuration of the phase leg for the four-level π-Type inverter is illustrated in Fig. 1, comprising six switching devices from T_1 to T_5. It should be noted that T_1 - T_2, T_3 - T_4, and T_5 - T_6 are operated in complementary pairs. Table 1 lists the switching states, with E being the nominal voltage of the three DC-link capacitors. In the DC-Link, there are two junctions, N1 and N2. The junction currents flowing from these points, labeled as $i_{J1,x}$ and $i_{J2,x}$, are determined by the phase load current, $i_{o,x}$, along with the switching states, subscript symbol *x* denotes phase *a*, *b*, or *c*.

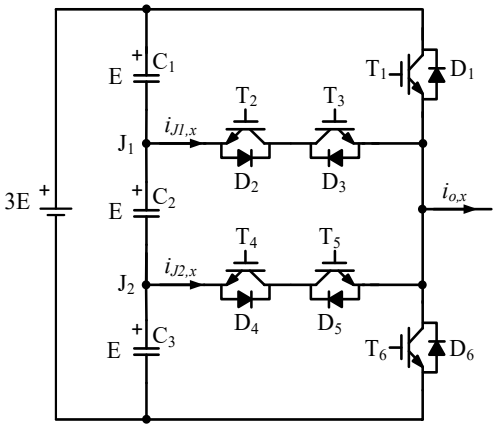


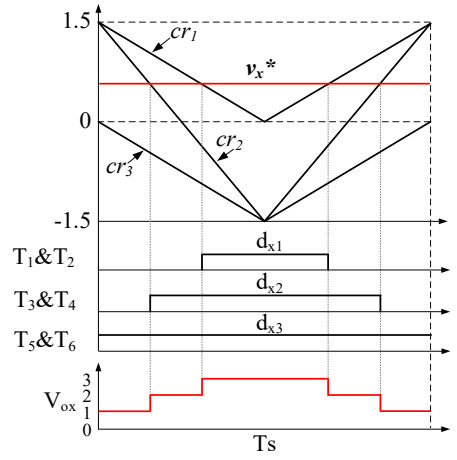
Fig. 1. Single phase circuit of 4L π-Type inverter.

Table 1. Switching states of 4L π-Type inverter

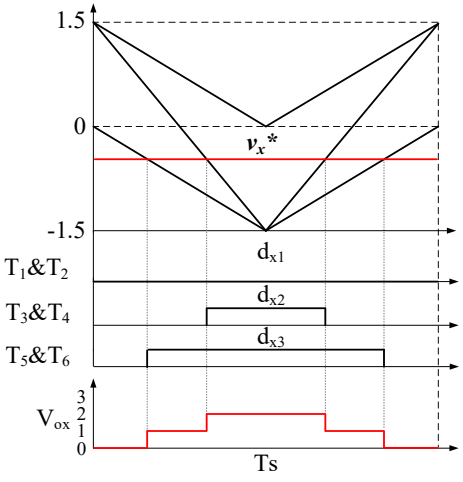
T1& T2	T3& T4	T5& T6	Switching states	vox	iJ1,x	iJ2,x
1	1	1	V3	3E	-	-
0	1	1	V2	2E	i0,x	-
0	0	1	V1	E	-	i0,x
0	0	0	V0	0	-	-

2.2. COPWM Modulation

Fig. 2 displays a diagram of the COPWM approach for the 4L inverter. Carrier Cr_2 overlaps both Cr_1 and Cr_3 with a peak-to-peak value of 3, while carriers Cr_1 and Cr_3 are level shifted, with Cr_1 put in the positive voltage zone and Cr_3 in the negative voltage region.



(a) Positive reference voltage



(b) Negative reference voltage

Fig. 2. COPWM modulation scheme for 4L π-Type.

The duty cycles generated by these carriers can be represented as functions of the phase reference voltage using this COPWM approach as follows:

1) When the reference voltage v^* is positive and intersects carriers Cr_1 and Cr_2:

$$d_{x1} = 2/3 \cdot v_x^*;\ d_{x2} = 1/3 \cdot \left(v_x^* + 1.5\right);\ d_{x3} = 1. \quad (1)$$

2) When the reference voltage v^* is negative and intersects carriers Cr_2 and Cr_3:

$$d_{x1} = 0;\ d_{x2} = 1/3 \cdot \left(v_x^* + 1.5\right);\ d_{x3} = 2/3 \cdot \left(v_x^* + 1.5\right). \quad (2)$$

According to Table 1, the junction current at N1 corresponds to the phase load current when the pole voltage is 2E, and the junction current at N2 corresponds to the phase load current when the voltage level is E. Referring to

Fig. 2, the following can be used to express the single-phase junction currents throughout a sampling period:

$$I_{J1,x} = d_{x2} - d_{x1} = \begin{cases} 1/3 \cdot \left(-v_x^* + 1.5\right) \cdot i_{0,x} & 0 \le v_x^* \le 1.5 \\ 1/3 \cdot \left(v_x^* + 1.5\right) \cdot i_{0,x} & -1.5 \le v_x^* \le 0 \end{cases} \quad (3)$$

$$I_{J2,x} = d_{x3} - d_{x2} = \begin{cases} 1/3 \cdot \left(-v_x^* + 1.5\right) \cdot i_{0,x} & 0 \le v_x^* \le 1.5 \\ 1/3 \cdot \left(v_x^* + 1.5\right) \cdot i_{0,x} & -1.5 \le v_x^* \le 0 \end{cases} \quad (4)$$

Assuming the capacitance of the DC-link capacitors is the same, denoted as C_0, the voltage errors of these capacitors caused by single phase junction currents in a carrier period can be expressed as follows:

$$\Delta v_{C1,x} = \frac{1}{3C_0}\left(2I_{J1,x} + I_{J2,x}\right)T_s \quad (5)$$

$$\Delta v_{C2,x} = -\frac{1}{3C_0}\left(I_{J1,x} - I_{J2,x}\right)T_s \quad (6)$$

$$\Delta v_{C3,x} = \frac{1}{3C_0}\left(-I_{J1,x} - 2I_{J2,x}\right)T_s \quad (7)$$

Under ideal and constant conditions, the middle DC-Link capacitor voltage can maintain balance in a carrier period since the difference between the two junction currents, as determined by formulas (3) and (4), is zero. According to (5) and (7), the voltage difference between the top and bottom capacitors caused by a phase leg depends on the total of two junction currents, which can be expressed as follows:

$$\Delta v_{C1,x} - \Delta v_{C3x} = \frac{1}{C_0}\left(I_{J1,x} + I_{J2,x}\right)T_s \quad (8)$$

The total junction current can be derived from (3) and (4):

$$I_{J1-2,x} = I_{J1,x} + I_{J2,x} = \begin{cases} 2/3 \cdot \left(-v_x^* + 1.5\right) \cdot i_{0,x} & 0 \le v_x^* \le 1.5 \\ 2/3 \cdot \left(v_x^* + 1.5\right) \cdot i_{0,x} & -1.5 \le v_x^* \le 0 \end{cases} \quad (9)$$

In the fundamental period, assuming that the reference voltage and load current are sinusoidal and symmetrical, the total junction current is zero. It has been demonstrated that, under ideal conditions, The top and bottom capacitors' natural voltage balance can be achieved via the COPWM, with the same outcomes attained for NPC [16].

2.3. Capacitor Voltage Balancing Control

Under ideal conditions, COPWM can naturally balance the voltages of the DC-link capacitors; but, if it is not properly controlled in nonideal or dynamic scenarios, it may become unstable. Therefore, to efficiently maintain the capacitor voltages, a capacitor voltage controller has been developed.

According to (8), to reduce the voltage variation of the top and bottom capacitors during a sampling interval, a reference value of total junction crrent needs to be injected into N1 and N2. This can be expressed as follows:

$$I_{J,ref} = -\frac{C_0 \cdot \left(v_{C1} - v_{C3}\right)}{T_s} \quad (10)$$

Since the total junction current depends on the reference voltage, the conventional ZSV injection method can modify the reference signal shape, thereby altering the junction current. However, calculating the optimal ZSV needed to produce the exact directly total junction current is challenging. For simplicity, only five key zero-sequence voltages (ZSVs) are considered, which clamp any reference voltage to -1.5, 0, or 1.5, and are denoted as $uz[j]$ (where j ranges from 0 to 5).

$$\begin{aligned} &uz[0] = 0; uz[1] = 3 - v_{\max}^*; uz[2] = 1.5 - v_{\max}^* \\ &uz[3] = 1.5 - v_{mid}^*; uz[4] = 1.5 - v_{\min}^*; uz[5] = 0 - v_{\min}^* \end{aligned} \quad (11)$$

where, $v_{\max}^*$, v_{mid}^* ,and $v_{\min}^*$ are the initial three-phase reference voltages' maximum, median, and maximal values. After injecting ZSVs, the changed reference voltage is described as follows:

$$v_{x,\mathrm{mod}}^*[j] = v_x^* + uz[j] \quad (12)$$

Next, by using equation (9), the corresponding total junction currents for these important ZSVs are determined. and compared with the required value. The most appropriate ZSV is determined by selecting the one that produces the total junction current in that is closest to the needed current in (10). To prevent overmodulation, the limit for ZSVs can be determined:

$$\begin{cases} u_{z\max} = 1.5 - v_{\max}^* \\ u_{z\min} = -1.5 - v_{\min}^* \end{cases} \quad (11)$$

As previously mentioned, the difference between the two junction currents affects the middle DC-Link capacitor voltage, which can be expressed as follows:

$$I_{J1,x} - I_{J2,x} = \left(-d_{x1} + 2d_{x2} - d_{x3}\right) \cdot i_{o,x} \quad (12)$$

If there is a voltage variation in the capacitor C2, the duty cycles of the switching signal d_{x1} , d_{x2} , and d_{x3} can be slightly adjusted to achieve voltage balancing under COPWM. A PI regulator takes Δv_{C2} to produce a duty ratio offset Δd. Consider the scenario where Δv_{C2} and $i_{o,x}$ are positive: the difference between the two junction currents must be positive to discharge the capacitor. If the reference voltage is positive, Δd be added to d_{x2} and subtracted from d_{x1} . Conversely, if the reference voltage is negative, Δd be added to d_{x2} and subtracted from d_{x3} . The generated voltage changes after adjusting duty cycles are illustrated in Fig. 3. The block diagram for capacitor voltage control is depicted

in Fig. 4.

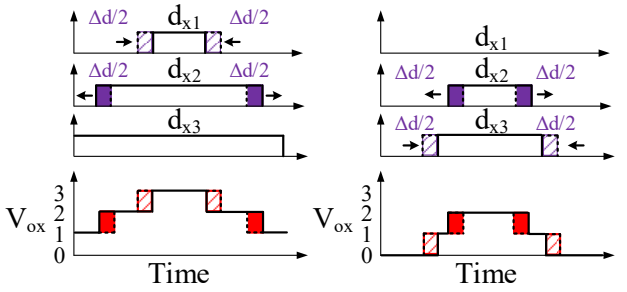


Fig. 3. Middle dc-link capacitor voltage balance method where Δv_{C2} and $i_{o,x}$ are positive.

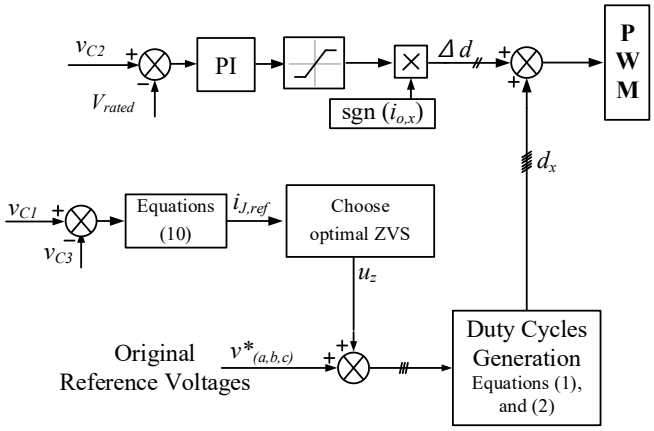


Fig. 4. Capacitor voltage control block diagram.

3. SIMULATION RESULTS

The performance of both the voltage balancing control and the PWM approach is demonstrated by the simulation results. The inverter parameters for the simulation are provided in Table 2.

Fig. 5 illustrates the steady-state performance of the inverter with a high-power factor *R-L* load, showing a power factor (PF) of 0.998 at a unity modulation index, as specified in the parameters table. The pole voltage, line-to-line voltage, load currents are shown in Fig. 5(a), (b), and (c), respectively. As depicted in Fig. 5d, the three DC-link capacitor voltages remained well-balanced under high power factor and high modulation index conditions. In contrast, with the traditional PWM method, voltage balance cannot be maintained for high power factors when the modulation index exceeds 0.55 [10]. The modified reference voltages after adding ZSV component are shown in Fig. 5e.

The steady-state performance of the inverter under a purely inductance load with m = 1.0 (R = 0 Ω, L = 30 mH) is displayed in Fig. 6. The results of the simulation demonstrate that voltages in all capacitors can be well controlled at both low- and high-power factors.

Furthermore, Fig. 7 displays the steady-state simulation result at the fundamental frequency of 1 Hz with a unity modulation index to demonstrate how well voltage balancing works in the case of low fundamental frequency. The capacitor voltage V_{c2} remained well-balanced at the rated value, while the top and bottom capacitors experienced larger voltage fluctuations. However, the voltage ripple in two capacitors is still within acceptable range $(\pm 10\%)$.

Table 2. Circuit parameters for the simulation

Parameters	Symbols	Values
Power rating	S_{rated}	3 kVA
DC source voltage	V_{dc}	240 V
Line-to-line voltage	$V_{l\text{-}l}$	170V
Fundamental frequency	f_o	50 Hz
DC-Link capacitor	C_0	2 mF
Carrier frequency	f_{sw}	2 kHz
R-L Load		10 Ω, 2 mH

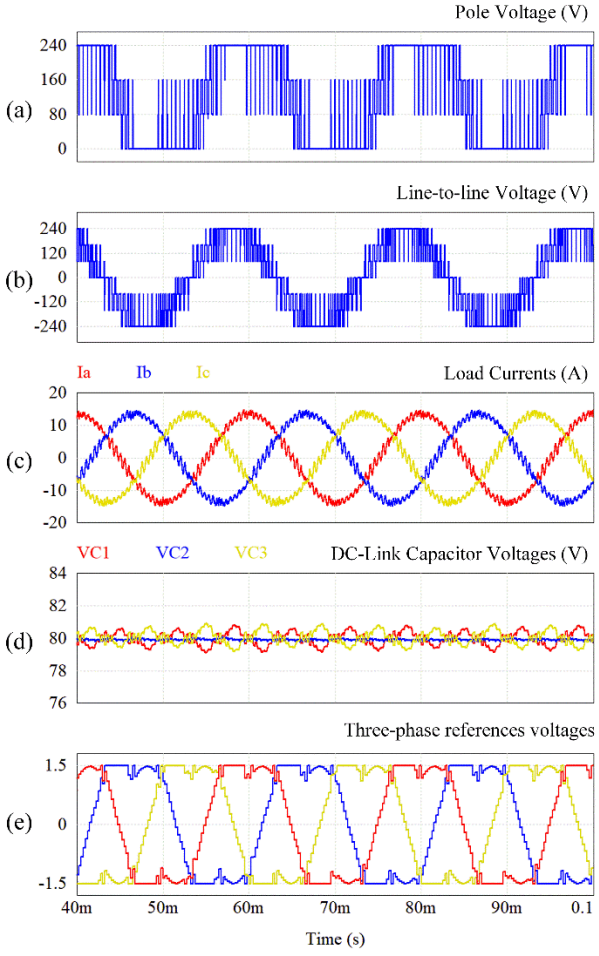


Fig. 5. Performance under high power factor and unity modulation index condition (m = 1.0, PF = 0.998).

The PWM method and voltage controllers have been verified in various dynamic conditions. Fig. 8 shows the simulation results when the modulation index changes in 0.2 steps, increasing from 0.2 to 1.0. The waveforms of the line-to-line voltage, phase currents, and DC-link capacitor voltages under LSPWM with modulation indices of $m = 0.5$ and $m = 0.7$ are displayed in Figs. 9 to confirm the performance of the COPWM in comparison to the conventional LS PWM. At a modulation index of 0.5, the LSPWM and zero-sequence-voltage injection method effectively equalizes the three DC-link capacitor voltages. However, increasing the modulation index to 0.7 disrupts this balance.

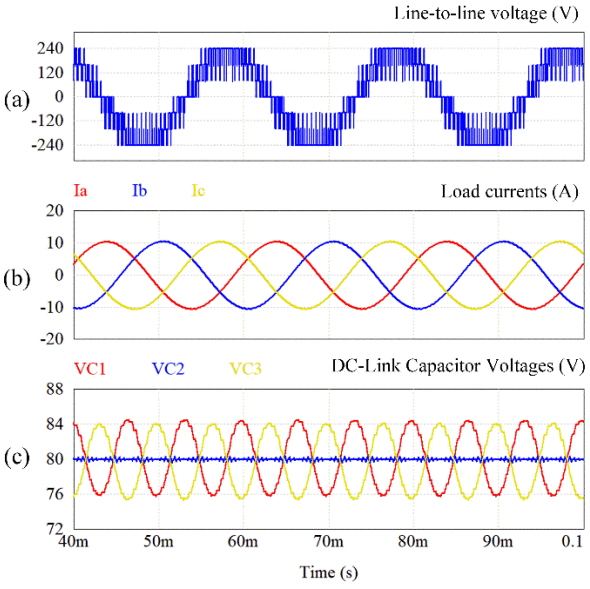


Fig. 6. Performance under pure inductance load and unity modulation index condition.

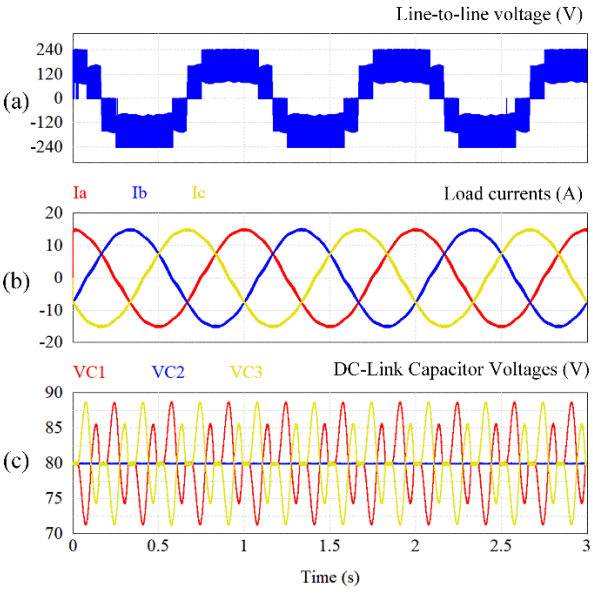


Fig. 7. Performance under low fundamental frequency operation.

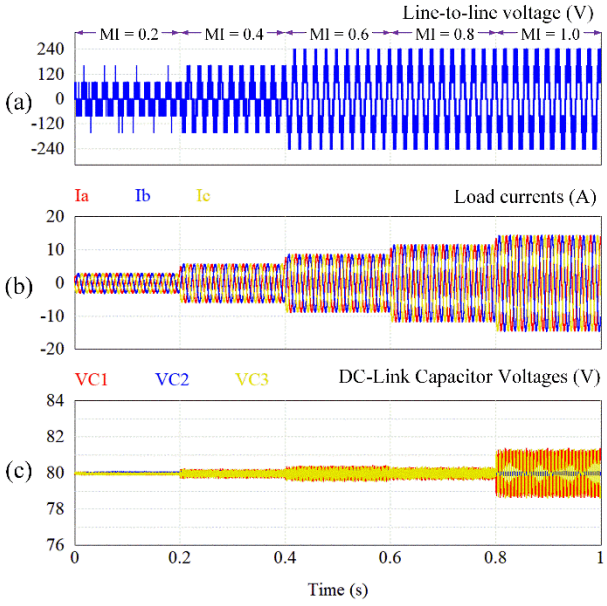


Fig. 8. Performance under a step change in modulation index.

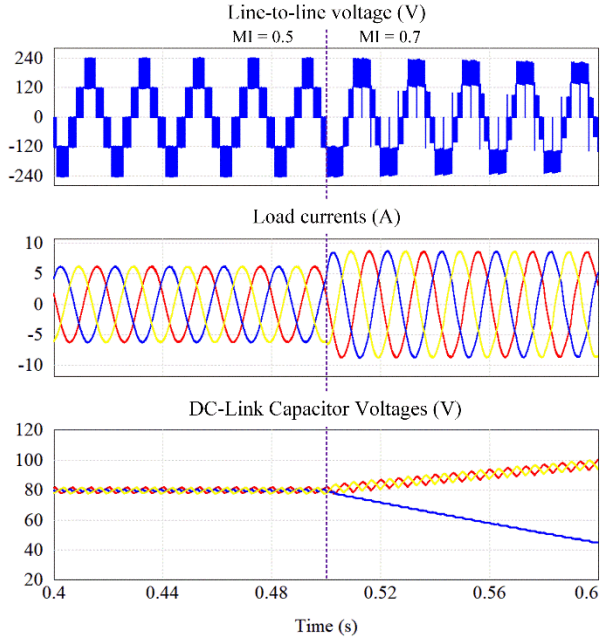


Fig. 9 Performance under LSPWM for a step change in modulation index (0.5 to 0.7).

The performance under variable voltage variable frequency (VVVF) is illustrated in Fig. 10. In two seconds, the modulation index increases uniformly from 0 to 1, while the fundamental frequency increases correspondingly from 0 to 50 Hz. It is evident that the three capacitor voltages can be maintained throughout the entire modulation index range.

The performance of the inverter has been tested under step load conditions while operating at 50 Hz fundamental frequency and unity modulation index. Initially, the 4L π-type is operated around 20% rated power and then, the load is changed to the rated value at t = 0.2 s. At t = 0.4 s, the load

steps down from full load back to 20 %. As shown in Fig. 11, in both cases, the maximum deviation voltage of DC-link capacitors during the transient period is approximately 5 % of the nominal voltage (4 V).

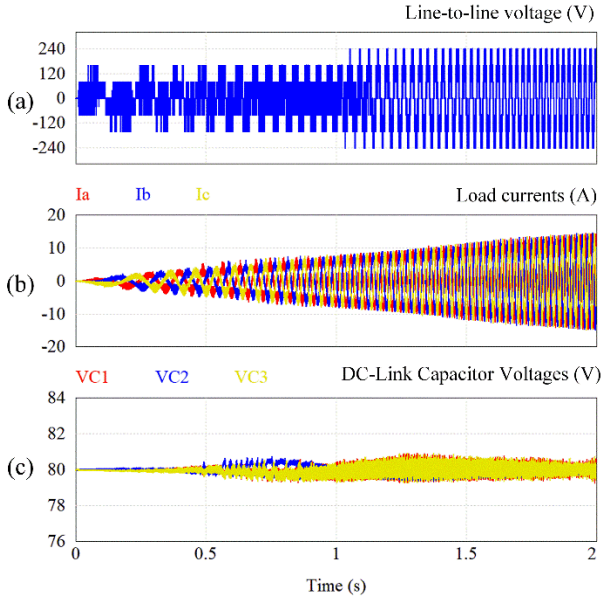


Fig. 10. Performance under variable voltage variable frequency VVVF operation.

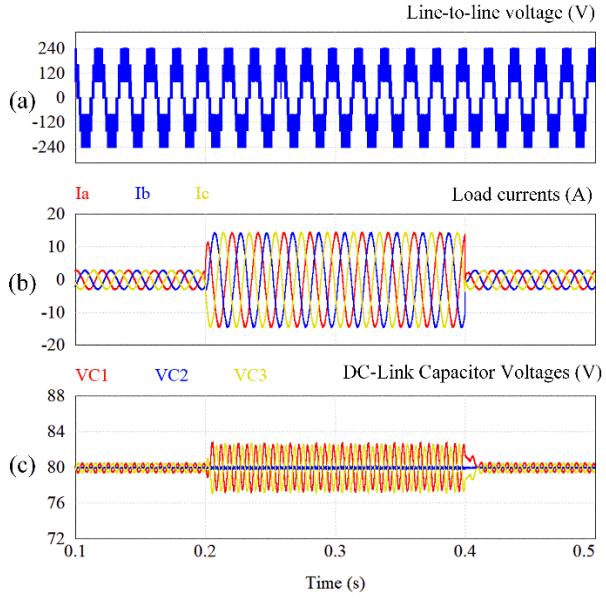


Fig. 11. Performance at the transient load condition.

4. CONCLUSIONS

Originally developed for NPC prototypes, COPWM has been successfully applied to the 4L π-type inverter, offering greater flexibility in achieving various control objectives, such as maintaining capacitor voltage balance. Under PWM control, natural voltage balancing of all DC-link capacitors is achieved under ideal steady-state conditions. However, to address voltage deviations caused by nonideal factors, a capacitor voltage control strategy is employed. This strategy involves zero-sequence voltage injection to balance the upper and lower DC-link capacitor voltages and adjusting the duty cycles of switching signals to balance the central DC-link capacitor voltage. The effectiveness of the COPWM method in the 4L π-type has been confirmed by simulation studies, indicating that PWM is an effective technique for ensuring capacitor voltage balance throughout all operating areas without requiring additional circuits.

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