



# Analysis of Higher Voltage Gain Switched-Capacitor-Based Boost MLI Topology

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## ABSTRACT

This paper presents an innovative switch capacitor-based multilevel inverter topology that utilizes a single input DC voltage source, particularly suitable for low-voltage renewable energy applications. That design incurred to the capacitor and 12 switches allowing for a remarkable triple voltage gain and the seven-level output voltage across the load. This topology is that it can effectively address the challenges associated with the best voltage balancing. The equivalent circuit analysis reveals that the capacitor charge operates in parallel with the DC source enabling them to nearly match the input voltage level. Furthermore, the paper introduced are generalized structure for the seven levels enhancing its applicability in various contexts. In the modernized world DC-AC converters, commonly referred to as inverters are essential components in generating, transmitting, distributing, and consuming electric power. A crucial role in a wide range of application, including medium and high voltage DC power transmission air conditioning system utilization of DC power sources such as solar cells and wind turbines, and until interruptible power supplies. The advancement in inverter topology presence in this paper is virtual for the ongoing transmission to worse sustainable energy suitable solution.

## 1. INTRODUCTION

Multilevel converters utilize a substantial number of switches to convert input DC voltage into stepped AC voltage. This approach has several advantages over 2-level power converters. Stepped voltage can achieve higher-quality waveforms [1]. Using smaller voltage steps also reduces  $dv/dt$  stress, thereby alleviating electromagnetic compatibility concerns. Multilevel converters have series semiconductor connections that allow for higher voltage operations [2]. Clamping diodes are used in series to eliminate overvoltage issues. Synchronize the switching of these switches to reduce switching frequency and minimize switching losses. Multi-level inverters (MLI) require a large number of switches. MLIs can use low-voltage rating switches, which makes the cost of an active semiconductor comparable to that of a 2-level converter [3]. However, the addition of the required gate-driving circuitry complicates the mechanical layout of the converter. MLI is the need for a collection of isolated or series capacitors to produce small voltage steps. The availability of voltage sources (VS) can pose an issue, and a voltage balance is required for series capacitors [4]. Because there are so many semiconductor devices, reducing the switch state can be used to solve the voltage balancing problem. Though another multilevel converter might be required to completely solve the voltage-

balancing issue, multilevel converters gained popularity because of their high efficiency, high-quality power output, and reduced total harmonic distortion (THD) [5], [6] MLIs, in addition to the previously mentioned benefits, ensure the reduction of filter components and electromagnetic compatibility issues.

The no. of DC source used has led to the proposal of numerous MLI topologies are shown in Figure 1. Common DC-source-based MLIs include diode-clamping and flying capacitor MLIs [7]. Cascaded H-bridge, hybrid cascaded H-bridge, and switched capacitor MLIs use separate DC sources for output voltage levels [8]. Researchers have said that they can control the MLI output voltage using different types of pulse width modulation (PWM) [9]. Such as sinusoidal PWM, spatial vector modulation, pulse amplitude modulation, selective harmonic elimination PWM, and selective harmonic mitigation PWM [10]. The state of MLIs, their structures, and PWM schemes. MLIs are increasingly popular in the industry for power electronic conversion in high-power applications, with two-level inverters being the most commonly used for electric vehicle applications [11]. However, studies and research have shown that MLI can be cost-effective and improve power quality within acceptable standards. MLIs can increase output voltage levels in steps with the addition of a few extra components [12].

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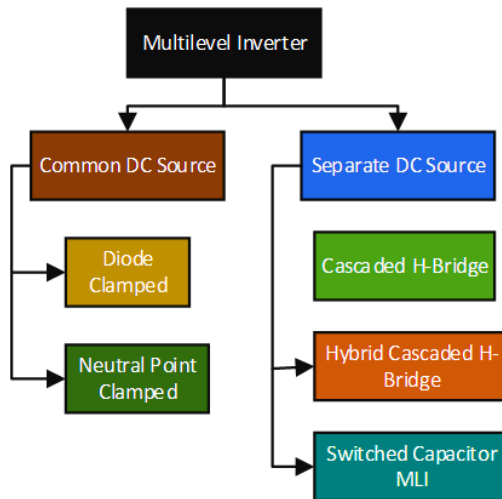


Fig. 1. Different Types of MLIs.

The objective of the paper is to introduce a switched capacitor-based MLI topology that improves efficiency, reliability, and suitability for modern renewable energy systems. The device aims to archive a triple voltage gain from a single input DC voltage source, resulting in a 7-level output voltage across the load. Capacitor voltage balancing improves system reliability and performance without complex external balancing mechanisms. Component-count reduction is achieved by using fewer switches and eliminating the need for diodes. Low voltage stress extends their lifespan and enhances the durability of the inverters. The generalized topology structure offers flexibility for designing MLI for various configurations and use cases.

The manuscript is organized as follows: (1) This section provides a detailed introduction, study of MLIs, objectives, and outline of the paper. (2) This section provides a detail of different types of basic converters. (3) This section provides a detailed application of inverters based on block connections. (4) This section provides details of inverter topologies using switching conducting modes. (5) This section provides a PWM for MLIs. (6) This section provides a detail of different switched capacitors based on boost MLIs. (7) This section provides a result. (8) This section provides a summary of the completed work, as well as suggestions for further work.

**2. BASIC CONVERTERS**

**2.1 Convectional 2-Level Inverter**

The development of the conventional 2-level inverter primarily aimed to convert DC voltage to AC voltage, as shown in Figure 2. These inverters provide only two-level outputs, namely  $-\frac{V_{dc}}{2}$  and  $+\frac{V_{dc}}{2}$ , where  $V_{dc}$  is the DC voltage input. PWM switches between these voltages to achieve the desired AC output voltage shown in Figure 3. This is a simple and effective way to generate an AC volt output from a DC input voltage. However, this generates

high  $\frac{dv}{dt}$  and harmonic distortions in the output. This converter is not preferred because mostly output voltage with low distortion is preferred; however, it laid the groundwork for MLI [13].

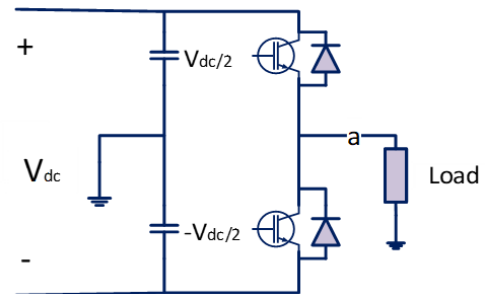


Fig. 2. Two-Level Inverter with Waveform without PWM.

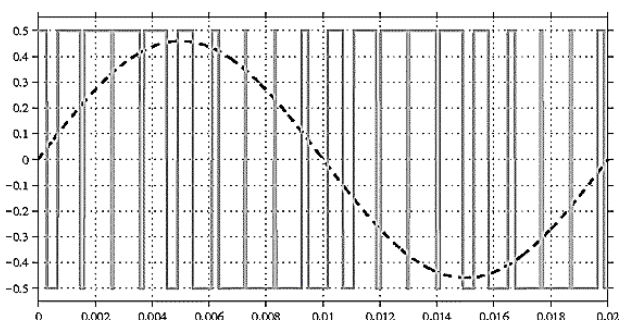


Fig. 3. PWM Voltage Output Reference Sine Wave.

**2.2 Convectional Three-Level Inverter**

A 3-level inverter is more effective and gets around some of the challenges of a 2-level inverter [14]. The inverter's H-bridge layout of three switches enables it to generate three voltage levels: positive, zero, and negative [15]. A frequency and waveform that correspond to the AC grid can be produced by the 3-level inverter by turning the three switches on and off at a high frequency [16]. Also can produce higher voltage levels using PWM, producing a voltage output that is twice that of the DC voltage source [17]. The changes between a two-level and three-level inverter are displayed in Table 1.

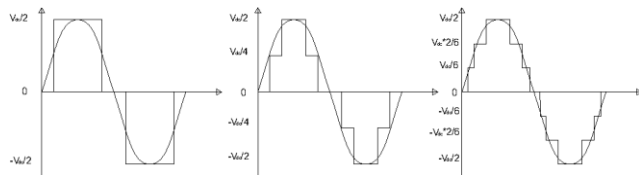
Table 1. Differences between a 2-3 level inverter

<b>o/p V-Levels</b>	The output voltage waveform of a 2-level inverter alternates between two voltage levels, whereas a 3-level inverter alternates between three voltage levels, usually +Vdc, 0V, and -Vdc.
<b>Harmonic Distortion</b>	A 2-level inverter's limited output voltage levels result in increased harmonic distortion. However, the performance and efficiency of a 3-level inverter with extra voltage levels are enhanced by reduced distortion.

<b>Switching Frequency</b>	A 2-level inverter cannot provide the same output waveform as a 3-level inverter without a greater switching frequency because of its staircase-like output waveform.
<b>Topology</b>	The topology of two-level inverters is simpler; However, the circuits of three-level inverters are more intricate, containing more switching components and capacitors.
<b>o/p voltage waveforms</b>	The output voltage waveform from two-level inverters is square, whereas the output voltage waveform from three-level inverters is sinusoidal and has less harmonic distortion.
<b>Efficiency</b>	In general, 3-level inverters have higher efficiency compared to 2-level inverters because of their sinusoidal output voltage waveform and reduced harmonic distortion.
<b>Cost</b>	Three-level inverters are usually costlier because of their intricate topology and extra parts, compared to two-level inverters.
<b>Applications</b>	Low-power applications like lights and household appliances typically use 2-level inverters, However, high-power uses such as RE systems electric cars, and industrial motors are better suited for 3-level inverters.

**2.3 Concept of Multi-Level Inverter**

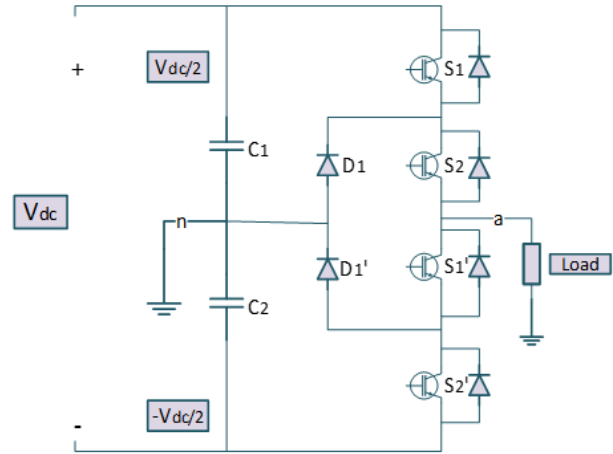
Figure 4 illustrates the construction of MLIs built to overcome the demerits of 2-level inverters of high total harmonic distortion and high  $\delta v$ . The idea of an MLI is to generate a smooth, stepped output. This reduces harmonic distortion and lowers  $\delta v$ . MLI consists of series-connected switches that switch at staggered frequencies and capacitor VS. Staggered switching helps to generate a smooth stepped output voltage and reach a higher level of voltage [18].



**Fig. 4. 3-Level, 5-Level, 7-Level Waveform.**

The output voltage becomes smoother with an increase in the number of voltage steps; the output voltage becomes smoother. However, the downside of this approach is that it increases the circuit's complexity, making control more difficult. A sample three-level inverter gives us a better understanding of the above statement. This type of inverter has three output voltage levels,  $-\frac{V_{dc}}{2}$ ,  $0$  and  $+\frac{V_{dc}}{2}$ . This inverter is almost identical to the 2-level inverter, except that

it has twice as many electrical components as the 2-level inverter and has a neutral or grounding point, as shown in Figure 5.



**Fig. 5. Single Phase Leg of 3-Level Inverter.**

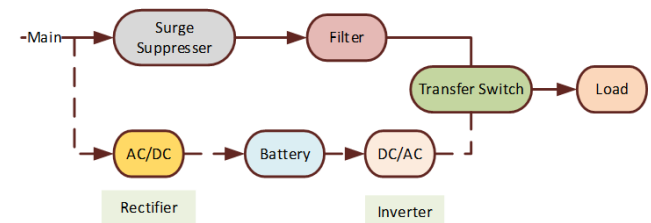
**3. APPLICATIONS OF INVERTER**

**3.1 Uninterruptible Power Supply**

Usually, power is stored in batteries, super capacitors, or flywheels in UPS. UPS can provide immediate protection from power interruptions. Generally, the stored power lasts for a short time; however, it is enough to safely shut down the machine [19]. UPS consists mainly of three types:

**3.1.1 Off-Line UPS**

The off-line UPS, also known as standby UPS, provides the most basic features. In this setup, the main line serves as the primary source, and in the event of a power outage, the switch automatically switches to a backup source [20], as shown in Figure 6.



**Fig. 6. Off- Line UPS.**

**3.1.2 On-Line UPS**

This type of UPS uses the double conversion method. An inverter rectifies the AC input from the mains into DC, stores it in the battery, and then converts it back to AC. Situations necessitate electrical isolation. During power outages, the rectifier serves no purpose; instead, the battery provides DC voltage, which the inverter transforms into AC voltage [21], as shown in Figure 7.

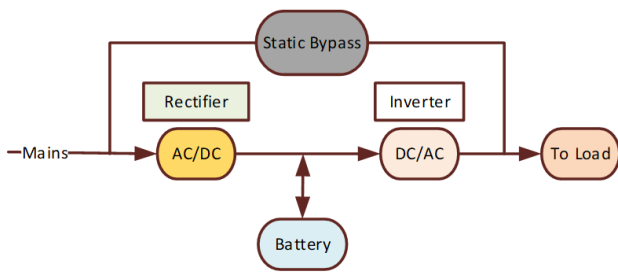


Fig. 7. On-Line UPS.

### 3.1.3 Line Interactive UPS

The line interactive UPS, similar to the offline UPS, connects to a tap-changing transformer. Depending on the input voltage, a tap-changing transformer regulates the voltage. The UPS incorporates additional filters to minimize transient loss [22], as shown in Figure 8.

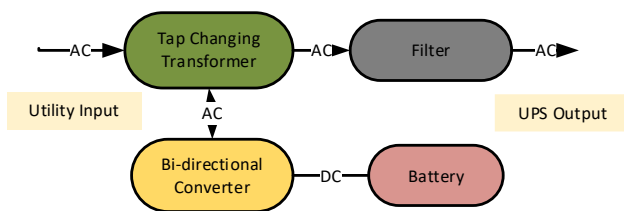


Fig. 8. Line Interactive UPS.

### 3.2 HVDC Transmission

Long-distance power transmission involves the use of HVDC transmission. This is a very efficient way to transfer power because it is less expensive and reduces heat losses during transmission. Another benefit of HVDC is that it can interconnect networks with different frequencies and natures. HVDC first converts power from AC to DC, transmits it, and then uses inverters at the load end to convert the DC back to AC [23], as shown in Figure 9.

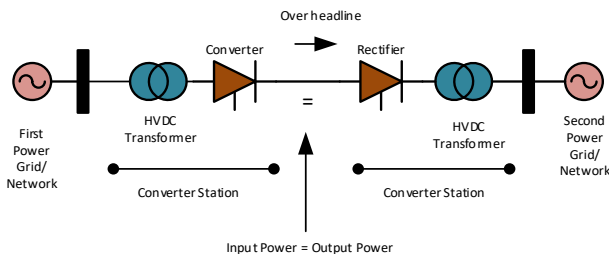


Fig. 9. HVDC Transmission Circuit.

### 3.3 Electric Drives

EVs and HEVs use MLI in the main traction drive. A multi-

level inverter offers multiple options, such as using low-voltage switching devices, using higher voltage, and maintaining the device's low switching frequency. These options contribute to enhancing the efficiency of electric vehicles. Additionally, inverters can regulate the frequency of AC output, thereby controlling the speed of motors [24].

### 4. INVERTER TOPOLOGIES

Different types of inverter topologies are available.

#### 4.1 Neutral Point Multi-Level Diode Clamped Inverter (NCPMLI)

This converter uses clamping diodes to produce stepped AC output through cascaded DC capacitors in various phases. The circuit's neutral point gave rise to the term "neutral point MLI. The converter finds its use in medium-voltage drives, which do not require switching devices in series [25]. This type of inverter reduces  $\frac{dv}{dt}$  values and produces less THD. For n-level output, the number of capacitors required in the series-connected DC link bus is  $n - 1$ . The series-connected capacitors divide the DC voltage, which the switches then receive. For n-level output, the total number of switches required is  $2 * (n - 1)$ . The switches are in complementary pairs. For n-level output,  $n - 2 * (n - 1)$ amping diodes are required [26]. For an n-level inverter,  $n - 1$  switching cells are required. Figure 10 shows that for a 5-level MLI, 4 cells are required. Cell 1 always has S4, S3, and S2 turned on. S1 and S5 are alternately switched. This produces output voltage levels of  $\frac{V_{dc}}{2}$  and  $\frac{V_{dc}}{4}$ , respectively. In cell 2, S5, S4, and S3 are always on. S2 and S6 are alternately switched. This creates  $V_{dc}/4$  and 0 output voltage levels, respectively. In cell 3, S6, S5, and S4 are always on. S3 and S7 are alternately switched. This produces output voltage levels of 0 and  $-\frac{V_{dc}}{4}$ , respectively. In cell 4, S7, S6, and S5 are always on. S4 and S8 are alternately switched. This produces output voltage levels of  $-\frac{V_{dc}}{4}$  and  $-\frac{V_{dc}}{2}$ , respectively. Table 2. shows the switching pattern of 5-level NCPMLI and CCMLI.

Table 2. Switch Patterns of 5 Level NCPMLI and CCMLI

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
Vdc/2	On	On	On	On	Off	Off	Off	Off
Vdc/4	Off	On	On	On	On	Off	Off	Off
Off	Off	Off	On	On	On	On	Off	Off
-Vdc/4	Off	Off	Off	On	On	On	On	On
-Vdc/2	Off	Off	Off	Off	On	On	On	On

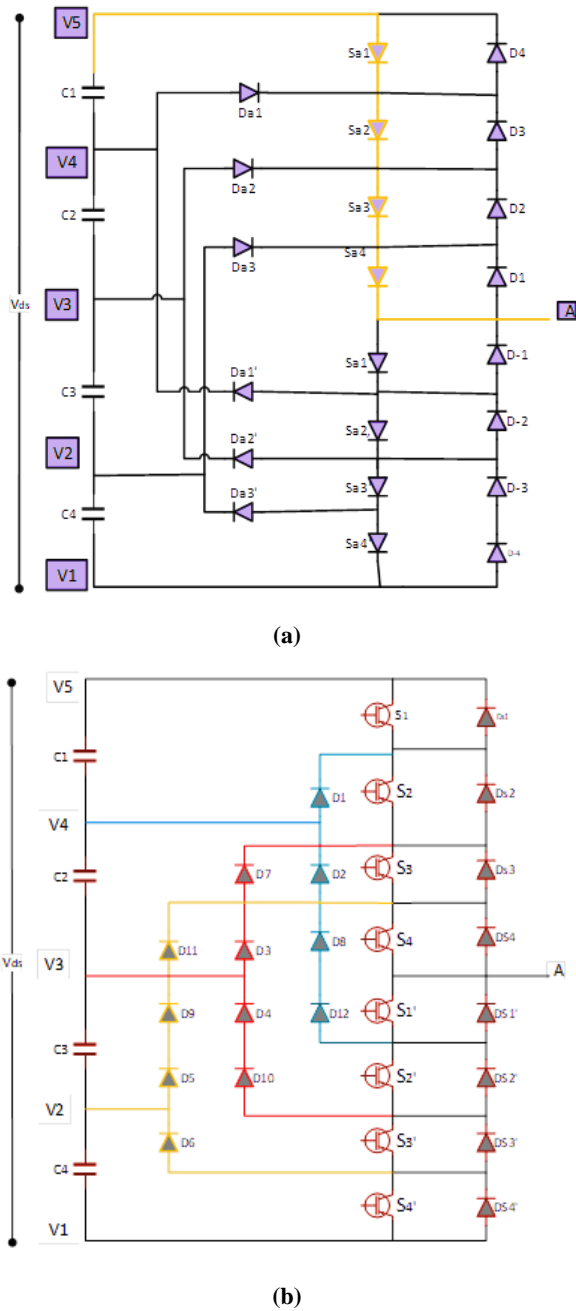


Fig. 10. Switching State of Five-Level NCPMLI.

4.2 Capacitor Clamped / Flying Capacitor MLI (CC/FC-MLI)

MLI is similar to diode-clamped MLI [27].

In Figure 11 topology, a capacitor controls the power device's voltage. We also use a capacitor to divide the voltage. Capacitors provide a natural voltage-balancing technique. A higher resistive load makes the flying capacitor's balancing faster [28].

Five voltage levels are displayed through the neutral point "n" in Table 3. It takes a few switching combustions to get to  $V_{an}$ . Voltage level  $V_{dc}/4$ , Switch S1-S4 is turned on for voltage  $V_{dc}/2$ , Three amalgamations are activated: 1)

S2, S3, S4, and S4'; 2) S2, S3, S4, and S4' ( $V_{dc}/4$  of C3's and  $(-V_{dc})/2$  of lower C4); 3) S1, S3, S4, and S3' ( $V_{dc}/2$  of top C4',  $(-3 V_{dc})/4$  of C3's or  $(-V_{dc})/2$  of C2); and voltage 0, S3, S4, S1', and S2'. All bottom switches S1' is active for voltage  $(-V_{dc})/2$ , and S1', S2', and S3' are triggered for voltage  $(-V_{dc})/4$  ( $V_{dc}/2$  of top C4's and  $(-3 V_{dc})/4$  of C3).

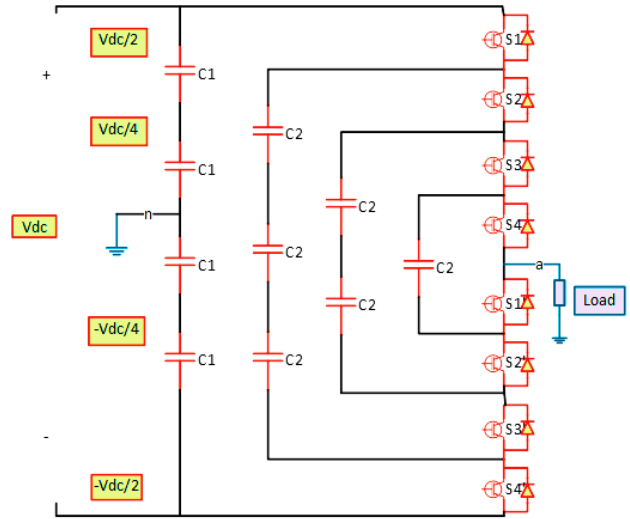


Fig. 11. Level FC-MLI.

Table 3. 5-Level FC-MLI Switching States

Voltage	G1	G2	G3	G4	G5	G6	G7	G8
$V_{dc}/2$	On	On	On	On	Off	Off	Off	Off
$V_{dc}/4$	On	On	On	Off	On	Off	Off	Off
Off	On	On	Off	Off	On	On	Off	Off
$-V_{dc}/4$	On	Off	Off	Off	On	On	On	Off
$-V_{dc}/2$	Off	Off	Off	Off	On	On	On	On

4.3 Cascade H-Bridge MLI (CH-B-MLI)

Figure 12 illustrates a CH-BMLI, A series of single full bridge inverters with DC buses that determines the output voltage level. For 'n' full bridge inverters connected in series, the number of output voltage levels is  $2 * n + 1$ . Each full-bridge inverter has one DC source and can be producing 3V level:  $v_{cmc}$  0, and  $-v_{cmc}$ . The amplitude of the input voltage to each full-bridge inverter may be the same or different, depending on the required output [29].

The number of voltage levels for the complete bridge inverter linked in series is  $2 * S + 1$ . The input voltage of each full bridge inverter may be the same or different. Each full-bridge inverter can produce  $v_{cmc}$ ,  $0_{cmc}$  and  $-v_{cmc}$  voltages. If full bridge inverters are connected in series, then the maximum and minimum voltage output receivable will be  $S * V_{cmc}$  and  $-S * V_{cmc}$ , respectively. For 'n' voltage

levels,  $s = (n - \frac{1}{2})$  series connected full bridge inverters are required, and each full bridge inverter requires 4 diodes and 4 switches.

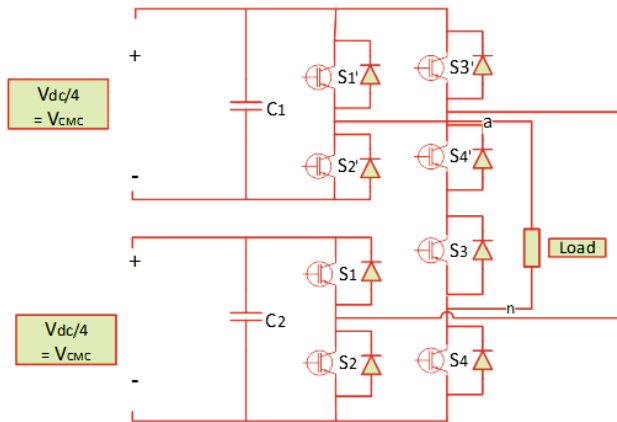


Fig. 12. 5-Level Cascaded H-Bridge MLI Circuit.

4.4 Generalized P2-Cell MLI (GP2-MLI)

Figure 13 shows that when transferring active power, CH-B-MLI, FC-MLI, and DC-MLI all face the issue of unbalancing. A generalized P2-cell multi-level inverter overcomes this problem as it can balance voltage itself, irrespective of inverter control and load characteristics. This type of topology can transfer both reactive and active power without the need for any extra circuits. Converted the generalized topology into NCPMLI, CC-MLI, C-MLI, and even conventional two-level inverters. We transformed the generalized topology into NCP-MLI, CC-MLI, C-MLI, and even traditional two-level inverters. Each P2 cell is independent and has two switch diodes and a lone DC capacitor. One switch on a P2 cell should turn off the other. Each capacitor is charged to  $V_{dc}/(n - 1)$  voltage where n is the output voltage levels. An n-level G-MLI, there must be  $\frac{n(n-1)}{2}$  P2 cells. When the quantity of output levels rises, the quantity of P2cells required increases quadratically. Table 4 display the P2-cell MLIs switching actions.

$$V_{out} = \sum_{i=1}^N V_i = \sum_{i=1}^N (S_i \cdot V) \tag{1}$$

$$V_{out} = (S_1 \cdot V) + (S_2 \cdot V) + (S_3 \cdot V) \tag{2}$$

4.5 Reversing Voltage MLI (RV-MLI)

Figure 14 shows that the first part controls voltage levels with a positive polarity. The other part controls polarity. Since voltage level switching occurs at a high frequency, the first part necessitates high-frequency switches. The other part works at a lower frequency since changes in polarity are less frequent, and thus this part requires switches that work at a lower frequency. The second part works at a fundamental frequency.

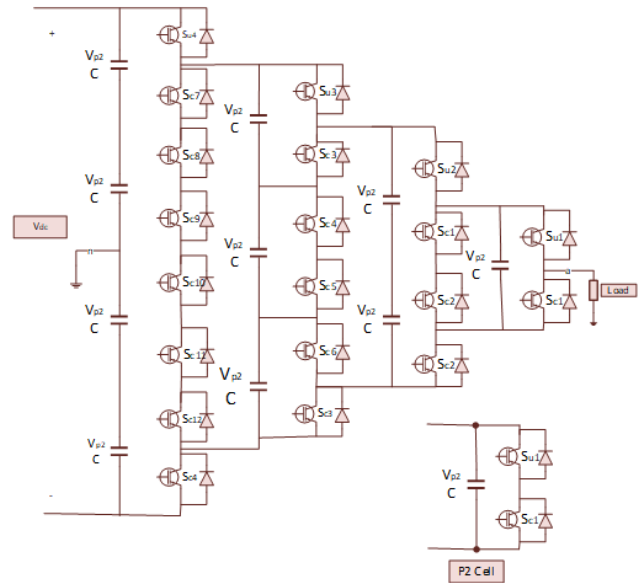


Fig. 13. 5 Level G-MLI and P2 Cell.

Table 4. Switching Pattern of P2-Cell MLIs

	0	V	2V	V	0	-V	-2V	-V
S1	On	On	On	On	On	Off	Off	Off
S2	On	Off	Off	Off	On	On	On	On
S3	Off	Off	Off	Off	Off	On	On	On
S4	Off	On	On	On	Off	Off	Off	Off
S5	On	On	On	On	On	On	Off	On
S6	On	On	Off	On	On	On	On	On
S7	Off	Off	Off	Off	Off	Off	On	Off
S8	Off	Off	On	Off	Off	Off	Off	Off

The inverter is composed of a voltage-level controlling part and a polarity-controlling part. The voltage-level controlling part operates at a high frequency. The polarity-controlling part works at a fundamental frequency that is relatively lower. There is no need for clamping diodes or flying capacitors. Table 5 uses n-level output; three (n - 1) diodes and main switch are required. For n-level output,  $(\frac{n-1}{2})$  isolated input sources are required [30]. In this topology, using separate sources eliminates the need for voltage balancing. As output levels increase, the required number of diodes and switches increases linearly, as illustrated in the block diagram in Figure 15.

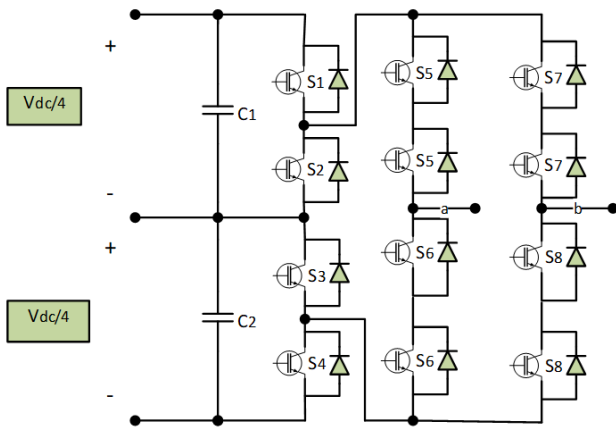


Fig. 14. 5-Level RV-MLI.

Table 5. Switching Pattern of 5-Level RV-MLI

o/p Voltage	S1	S2	S3	S4	S5	S6	S7	S8
Vdc/2	On	Off	Off	On	On	Off	Off	On
Vdc/4	Off	On	Off	On	On	Off	Off	On
Off	Off	On	On	Off	On	Off	Off	On
-Vdc/4	Off	On	Off	On	Off	On	On	Off
-Vdc/2	On	Off	Off	On	Off	On	On	Off

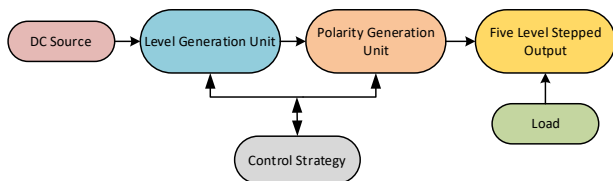


Fig. 15. Block Diagram of 5-Level RV- MLI.

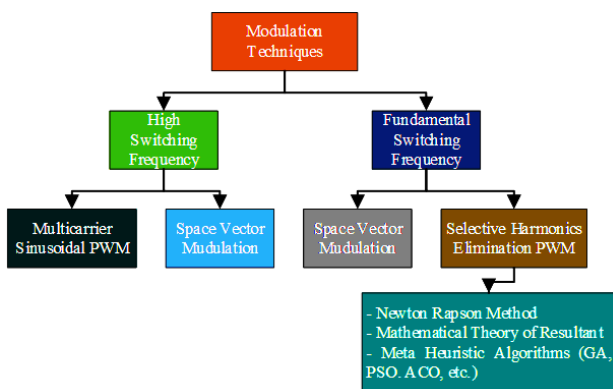


Fig. 16. Different Types of Modulation Techniques.

5. PWM FOR MLIS

In Figure 16 MLIs utilize PWM techniques to regulate output voltage and minimize distortion. High switching frequency PWM techniques include multicarrier sinusoidal

PWM and space vector PWM, whereas SVM and selected harmonics reduction PWM are basic switching frequency PWM strategies. These techniques are classified based on their switching frequency [31], [32]. Table 6 is showing the comparison of different MLI topologies.

Table 6. Caparison of Different MLI Topology

S. No.	Topology	Diode Clamped	Flying Capacitor	Cascade
1.	Power System	2(m-1)	2(m-1)	2(m-1)
2.	Diode Clamped for Each Phase	m-1, m-2	Off	Off
3.	Capacitor for DC-Bus	m-1	m-1	m-1/2
4.	Balanced Capacitor for each phase	Off	(m-1, m-2)/2	Off
5.	Unbalancing Voltage	Average	Higher	Very High
6.	Application	Systems for motor driving, STATCO M	STATCO M and the motor system	PV system, battery system, fuel cells, and motor drive system

6. SWITCHED CAPACITOR BASED BOOST MLI

This topic describes a multi-level inverter that uses a switched capacitor to boost its performance.

6.1 7- Level Boost Topology

Figure 17, the circuit diagram for the proposed MLI topology, shows that the circuit requires twelve unidirectional switches with opposite faces facing the same number of diodes. The structure of the set of diodes and switches makes the voltage flow unidirectional, while the current can flow in both directions. The circuit also consists of two capacitors and one DC voltage source. Both capacitors' voltage ratings are equal to the input voltage, Vdc. The input DC source could be anything, including renewable sources like fuel cells, batteries, photovoltaic cells, etc. This topology's voltage output can have seven levels: -3V<sub>DC</sub>, 3V<sub>DC</sub>, -2V<sub>DC</sub>, 2V<sub>DC</sub>, -V<sub>DC</sub>, V<sub>DC</sub>, and 0. At the voltage levels of -V<sub>DC</sub>, V<sub>DC</sub>, and 0, we connect the capacitors in parallel to each other, and subsequently, we connect both DC-VS in parallel to each capacitor [33]. These connection combinations result in capacitors charging up to V<sub>DC</sub> voltage. At voltage levels of -3V<sub>DC</sub> and 3V<sub>DC</sub>, we connect the capacitors in series and then in series with the DC

voltage source. At  $-2V_{DC}$  and  $2V_{DC}$  voltage levels, we connect the capacitors parallel to each other and then in series with the DC voltage source. The capacitors discharge as a result of these connection combinations that cause the

capacitors to discharge. Therefore, we observe that each cycle almost equally discharges and charges both capacitors [34].

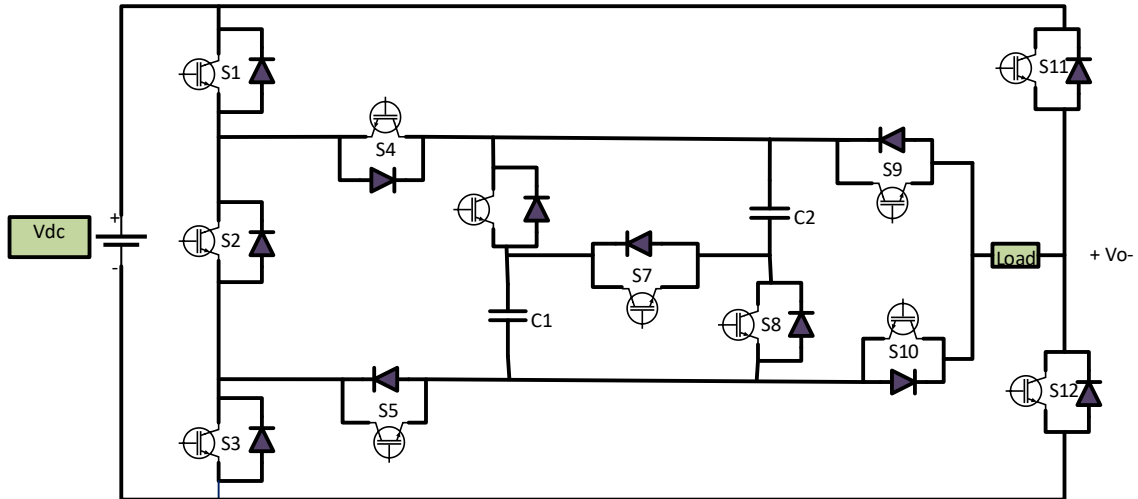


Fig. 17. 7-Level Switched Capacitor Based Boost MLI.

Table 7. Switching Pattern of 7-Level Boost Topology

S1, S8	S2	S3, S4	S6	S7	S8	S9	S10	S11	S12	Vc	Vc1	Vc2
On	On	Off	Off	On	Off	On	Off	Off	On	3Vdc	D	D
On	On	Off	On	Off	On	On	Off	Off	On	2Vdc	D	D
On	Off	On	On	Off	On	On	Off	Off	On	Vdc	C	C
On	Off	On	On	Off	On	Off	On	Off	On	Off	C	C
On	Off	On	On	Off	On	Off	On	On	Off	Vdc	C	C
Off	On	On	On	Off	On	Off	On	On	Off	-2Vdc	D	D
Off	On	On	Off	On	Off	Off	On	On	Off	-3Vdc	D	D

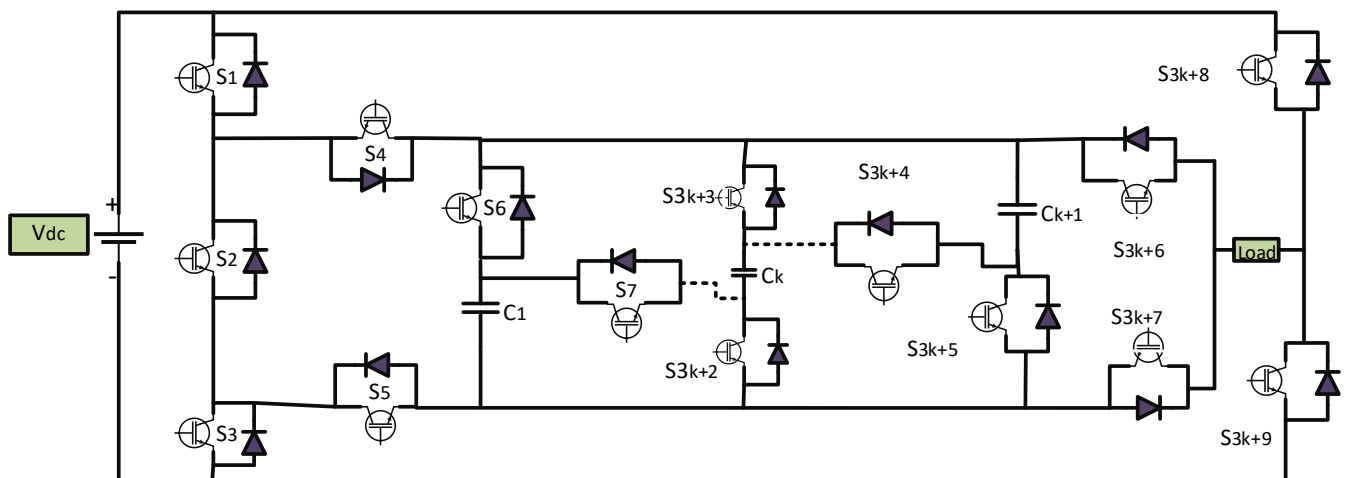


Fig. 18. Generalized Structure of Switch Capacitor-Based Boost Topology

**6.2 Switching State of 7-Level Boost Topology**

Table 7 shows that in this topology, the maximum voltage stress across the switches S4, S5, S9, and S10 is 2 volts. For the rest of the switches, the maximum voltage stress across them is  $V_{DC}$ , i.e., the maximum voltage they have to block is the same as the input voltage. The sum of the maximum voltage stresses across all the switches is known as the total standing voltage (TSV). TSV is equal to  $16V_{DC}$  for the 7-level boost topology.

To determine the output voltage of the 7-level boost topology, we can use the following equation:

$$V_0 = \left(\frac{S_{f1}+S_{f5}}{2}\right) + 2S_{f2} + \left(\frac{S_{f3}+S_{f4}}{2}\right) - \left(\frac{S_{f6}+S_{f7}}{2}\right) \left(\frac{S_{f9}+S_{f10}}{2}\right) - \left(\frac{S_{f11}+S_{f12}}{2}\right) + \left(\frac{S_{f8}+S_{f7}}{2}\right) 5(S_{f5} - S_{f11} - S_{f12}) - S_{f11} \quad (3)$$

Here,  $S_{fx}$  represents the switching function of the  $fx$  switch. It can take two values: 1 and 0.

**6.3 Generalized Structure of Switched Capacitor Based Boost MLI**

Figure 18 shows the addition of three switches and a capacitor to the 7-level boost. The MLI topology can increase two levels of output voltage while also increasing voltage gain. As a result, the number of output levels raises linearly with the numbers of switches and capacitors. [35]. We can calculate the required switches ( $N_{sw}$ ), voltage gain ( $G$ ), required capacitors ( $N_c$ ), and TSV using the following equations:

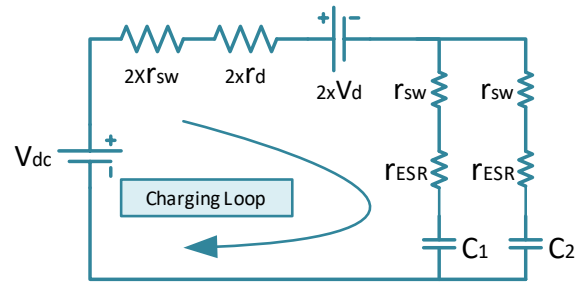
$$N_{sw} = \frac{3}{2}(N + 1), N_c = \frac{1}{2}(N - 3), G = \frac{1}{2}(N - 1) \quad (4)$$

$$TVS = 0.5 \times (7N - 17) \quad (5)$$

All the capacitors in the generalized structure have the same voltage rating as the input DC source ( $V_{DC}$ ).

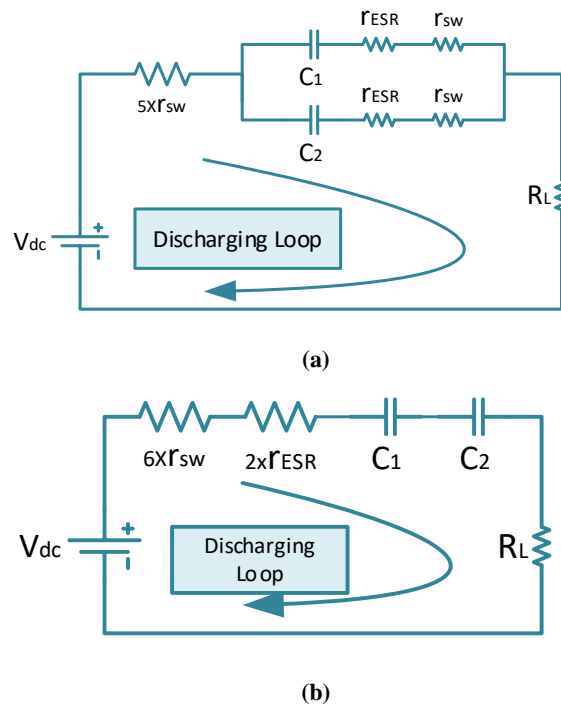
$$C_1 = C_2 = \frac{I_{pk}}{(\Delta V_C \times f_{sw})} \quad (6)$$

The proposed topology can self-balance the voltage in the capacitors. Figure 19 shows the charging loop of capacitors. It is the equivalent circuit for voltage levels  $0, +V_{dc}$  and  $-V_{dc}$ . The circuit connects both capacitors in parallel. The current path includes energy-dissipating switches and anti-parallel diodes. Represent the effective resistance of the switch as  $r_{sw}$  and the anti-parallel diode as  $r_d$ . The symbol  $r_{ESR}$  represents the capacitor's impedance. Due to the extremely low values of all the energy-dissipating elements, both capacitors nearly reach the input voltage level.



**Fig. 19. Equivalent Circuit at Voltages  $0, +V_{dc}, -V_{dc}$ .**

Figure 20 depicts discharging loops at voltage levels  $+2V_{dc}, -2V_{dc}$ , and  $+3V_{dc}, -3V_{dc}$ , respectively. According to the above figures, the charging loop has a lower time constant than the discharging loop, so charging occurs at a faster rate. Furthermore, in this topology, the charging loop balances the voltage drop during discharging, resulting in self-voltage balance.



**Fig. 20. Equivalent Circuit at Voltages Discharging Loop (a)  $+2V_{dc}, -2V_{dc}$  (b)  $+3V_{dc}, -3V_{dc}$**

The charging current is high in the charging loop because of the low impedance. Control the charging current's magnitude by adding a low-value inductor to the circuit. Use switches with higher current ratings in the charging loop. The variables  $r_{sw}$ ,  $r_{ESR}$ ,  $r_d$ , and  $V_d$  represent the switch's resistance during the ON state, the capacitor's equivalent series resistance, and the voltage drop across the diode, respectively.

### 7. RESULTS

Figure 21-23 is showing the switched capacitor-based boost MLI produces a five and seven-level output waveform with a maximum amplitude of three times the input DC voltage. Set the input DC voltage at 50V, and received a maximum output voltage of 150V. The voltage levels observed were 0V, 50V, 100V, 150V, -50V, -100V, and -150V. We rated the two capacitors at 2.2 mF. The rating of both capacitors was determined using,

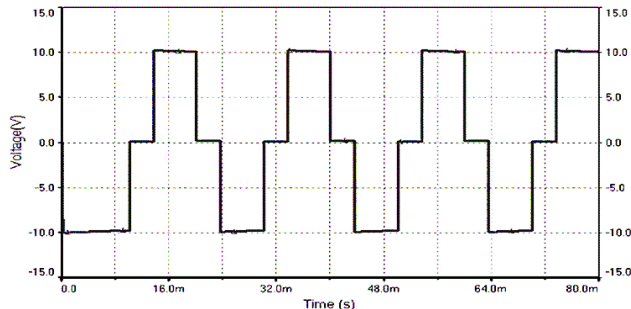


Fig. 21. Output Waveform of 5-Level NCPMLI.

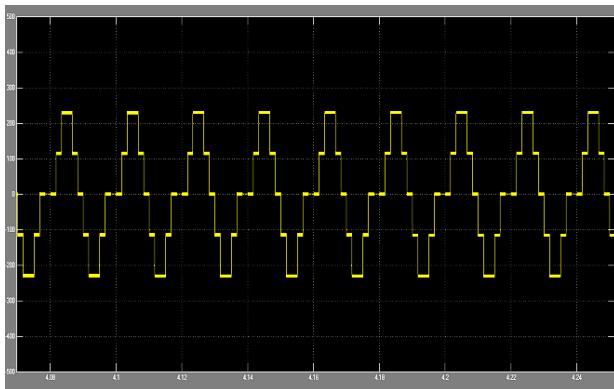


Fig. 22. Output Waveform of 5-Level CCMLI.

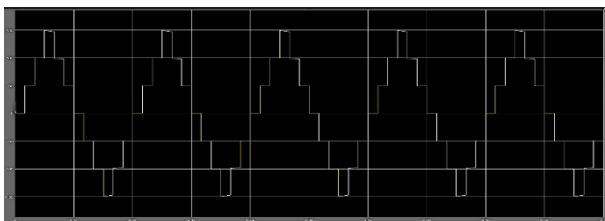


Fig. 23. 7-Level Output Waveform of Switched Capacitor-Based Boost MLI

### 8. CONCLUSION

MLI gained popularity because of their low dv/dt values and lower total harmonic distortion; traditional MLI, on the other hand, lacked some properties. Traditional converters can achieve high output levels using the required number of semiconductor devices. Additionally, the majority of renewable energy sources generate low-voltage output, which is insufficient to directly power high-voltage

appliances, necessitating the use of boost converters to meet this requirement. Additionally, some of the traditional converters encountered difficulties with charge balancing in their capacitors. The proposed topology overcomes the disadvantages listed above of traditional MLI while still possessing the basic features of MLI. The proposed topology boosts the output voltage by a factor of three. This topology can self-balance the capacitors and also requires a smaller number of switches and no diodes, therefore reducing losses. Thus, as the number of switches and increasing capacitors, so does the no. of output levels. The above-listed features of the switched capacitor-based boost MLI make it suitable for multi-proposal use.

#### Future Scope of MLIs:

- Renewable Energy Integration: MLIs are critical for incorporating renewable energy sources into the grid.
- Electric Vehicles (EVs): MLIs can manage power conversion between battery packs and motors in EVs.
- Grid-Tied Inverters: MLI topologies enhance the performance of grid-tied inverters.
- Energy Storage Systems (ESS): MLIs optimize energy storage systems by managing voltage conversion and minimizing losses.
- MLIs are ideal for microgrid applications that require a reliable power supply.
- Industrial Applications: MLIs provide clean, stable power to sensitive equipment.
- Smart Grid Technologies: MLIs support bidirectional power flow and integrate with advanced grid management systems.
- Research and Development: MLI technologies focus on efficiency improvement, cost reduction, scalability enhancement, and new topologies.

#### ABBREVIATIONS

- DC : Direct current
- AC : Alternat Current
- MLI : Multi-Level Inverter
- THD : Total Harmonic Distortion
- PWM : Pulse with Modulation
- UPS : Uninterruptible Power Supply
- HVDC : High Voltage DC Transmission
- D : Discharging
- C : Charging
- EV : Electric Vehicles
- HEV : Hybrid Electric Vehicles
- NCPMLI : Neutral Point Multi Level Diode Clamped Inverter
- CC/FC : Capacitor Clamped / Flying Capacitor

CH-B : Cascaded H-Bridge  
 GP2MLI : Generalized P2-Cell  
 RV-MLI : Reversing Voltage MLI  
 SVW : Space vector Modulation  
 TVS : Total Standing Voltage.

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