# A Self-Balancing Non-Isolated High-Gain 7-Level Inverter for Solar Photovoltaic Power Systems with Low Component Count

Neeraja B.[1], Dr. Sonal[2], Sonali R. Nandanwar[3], Rajender Boini[4], Addagatla Nagaraju[5,*], and Akkela Krishnaveni[6]

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ABSTRACT

This article presents a revolutionary DC voltage boost converter with a gain of nine times to its input. The main disadvantage of traditional Multilevel Inverter (MLI) is that, in order to use green energy sources, a high-voltage DC-DC chopper must be tolerant of raise input voltage. The suggested converter makes use of ten switches, two inductors, four diodes, three switching capacitors, and just one DC supply. The capacitor's voltage itself Self-Balancing automatically. with minimum no. of components including a capacitor is used to create the switched-capacitor (SC) multilevel-inverter (MI). To produce the output voltage waveforms with seven levels, the switching Inductor/capacitor must be appropriately charged and discharged. Without requiring a voltage regulating circuit with a closed loop, the suggested inverter can self-balance the capacitor's voltage. Because of the continuous series-parallel discharge and charging over a full cycle, three capacitors receive equal charges from the input source and the inductors. Compared to the majority of recently produced topologies, the suggested 7-level SC inverter involves fewer switches, driver diodes, capacitors, also semiconductor switches. Additionally, four pairs of switches run simultaneously using the same control signal, simplifying the control system, and eight of the ten the fundamental frequency is used by switches to function. The output of the inverter is controlled by a simple frequency switching scheme. On the PSIM/MATLAB platform, the suggested structure's voltage-boosting and self-balancing capabilities are verified.

## 1. INTRODUCTION

Because multilevel inverters offer a practical solution to voltage problems in high-power applications, they have completely changed the power electronics sector. High voltage has always been difficult to produce, but multilevel inverters have significantly altered the conventional method of producing boosted voltage waveforms [1]. The use of these inverters is growing quickly, and they are becoming more and more common in the commercial and industrial sectors [2]. Utilizing RES is becoming more widespread, as Reducing pollution and achieving carbon neutral emissions are the current global priorities. In order to achieve this goal, power converter research is necessary [3,4]. Recent years have seen study on a number of power converters, such as inverters that convert DC to AC and vice versa. The final approach to achieving this goal is the widespread use of multilevel inverters (MLIs) [5] Multilevel inverters (MLIs) are crucial converters from DC to AC at a time when renewable energy system installation is becoming more and more popular worldwide [6]. Renewable energy sources are perfect for creating numerous interconnected dc-links since they are often made up of several low-voltage DC sources, including battery backup systems, ultra-capacitors, and solar power cells. Hydrogen-based fuel cells, which are being researched for usage in energy-intensive applications, like onboard power systems, provide a similar situation [7].

Inverters with several levels were first proposed in the 1970s. It has been the subject of in-depth study and advancement ever since. These days, multilevel inverters are often utilized in numerous high-power applications, such as industrial drives, electric cars, and solar power [8]. Multilevel inverter technology has proven to hold the position of dependable and affordable way to produce top-notch results. low distortion in harmonic waveforms. The growing need for low distortion applications with high voltages has propelled the development of multilayer

[1]*Dept. of EEE, Government Polytechnic Nalgonda, Telangana, India.*
[2]*Birla Institute of Technology, Mesra Off-campus Deoghar, Jharkhand, India.*
[3]*Department of Electrical and Electronics Engineering IES College of Technology Bhopal*
[4]*Dept. of EEE, Chaitanya (Deemed to be University) Himayatnagar, Hyderabad, Telangana, India.*
[5]*Dept. of EEE, Government Polytechnic for Women, Siddipet, Telangana, India.*
[6]*Dept. of EEE, SRRS Government Polytechnic,Sircilla, Telangana, India.*
* *Corresponding author:* Addagatla Nagaraju; Email: Nagaraju.addagatla@gmail.com.

inverter technology [9]. For low-power applications, the traditional two-level inverter was the go-to option; however, it has drawbacks in activities involving high voltage. The dual-level inverter produces final products which have square waves with a lot of harmonic distortion, which leads to large losses and decreased efficiency. However, the multilayer inverter provides a solution to this issue by generating low distortions in the output waveforms, which lead to high efficiency and lower losses. Several levels of DC sources are combined by multilevel inverters in order to generate the intended output voltage waveform [10]. The number of DC sources and control mechanism employed in these topologies differ [11]. The clamped inverter with diodes clamps the output voltage using numerous diodes, On the other hand, the flying capacitor inverter stores energy in capacitors and adjusts voltage levels using them. To produce the required output waveform, the CHB converter employs several H-bridge modules, every one having an own DC supply [12, 13].

Reduced harmonic distortion, enhanced efficiency, enhanced dependability, and less strain on the power electronics components are some of these benefits [14]. Additionally, multilevel inverters provide better voltage and current waveforms, which lessen acoustic noise and electromagnetic interference. In the field of renewable energy, where high-voltage, low-distortion waveforms are essential, multilevel inverter technology has drawn a lot of attention [15]. It has been demonstrated that using multiple inverters in wind, solar, and other systems utilizing green energy improve the effectiveness and dependability of the process of power transformation. It has also been demonstrated that multilevel inverters improve the energy conversion mechanism's efficiency in electric vehicles, extending their range and cutting down on charging times [16]. An emerging technology in power electronics is the switched capacitor multilevel inverter (SCMLI), which transforms different amounts of AC voltage from DC voltage. Its numerous voltages of output are produced by a sequence of switched capacitor cells. An SCMLI's capacity to produce higher-quality waveforms as an output is one of its main advantages. This can be accomplished by the inverter using a range of voltage levels to mimic a sinusoidal waveform. Consequently, there is less distortion of harmonics, which is important in many applications including RES and motor control. Furthermore, the duty ratio for the switching signals can be changed by precisely control over output voltage, giving the load exact control. DC-AC conversion produced by MLIs can have high-voltage and power levels, additionally great efficiency. Among MLIs' characteristics include their smaller filter size, lower harmonic content, and lower individual device ratings. Previously, MLIs were implemented using “flying capacitor (FC), neutral point clamped (NPC), and cascaded H-bridge architectures (CHB)”. Higher level FC and NPC topologies contain significant counts of capacitors, which create problems with reliability and expense as well as demands for capacitor voltage balancing [17]. There have been several modified configurations created since their creation to get rid of their drawbacks. The three conventional topologies are beaten in component counts by the later created topologies. Aiming for Tolerance for defects, flexibility, efficiency, weight and volume constraints, researchers are currently creating MLIs using an application-based approach [18, 19]. The construction of buildings with fewer devices has been the subject of extensive effort [20, 21]. Comparably, researchers have also looked into device count optimization [22] and fault-tolerant decreased device count topologies [23]. Nevertheless, there are issues because a lot of DC sources are needed with control complexity and practical reality, particularly when using sources of renewable energy with varying voltage levels. First of all, the two traditional configurations—NPC and FC—are where capacitors are first seen in MLIs. Researchers' attention has recently been drawn to SCMLI-based topologies [24], which include series/parallel configurations of capacitors and switch modules, especially for applications where the ability to raise voltage is beneficial.

This boosting function allows for a considerable increase in low magnitude voltage, such as that of fuel cells or photovoltaic systems. This explains why boost dc/dc converters which are otherwise required as intermediary devices should be eliminated [25]. greatly lowering the size, effectiveness, and complexity of the generation system as a whole. However, efforts are currently being made to address the problems caused by the excessively high number of devices. It's interesting to note that [26] looks into replacing a CHB's many dc sources with capacitors, necessitating use just one DC source. With the use of one dc supply, two capacitors, nine switches, and a dual motivating element, the configuration suggested in [27] can produce a total of nine levels. One advantage of capacitor voltage self-balancing is that it does not require additional equipment or control circuitry. With a boosting factor of three, a configuration with two capacitors, one dc source, and three linked H-bridge structures can also generate seven levels [28]. In [29] the high number of parts may have a detrimental effect on the reliability of the system. [29] introduced an ANN-MPC based on the stability of Lyapunov and a seven-level improved PUC active rectifier built on floating weighting factor.

Due to their superior performance, SC based multilevel inverters (SC-MLI) are becoming increasingly essential when converting DC to AC electricity [30]. Better-performing electric vehicles & energy generated from renewable sources (RE) are added to the SC MLI configuration [31]. The structure is more appropriate for improving the power quality when multilayer inverters (MLI) generate a less distorted output voltage staircase pattern. The researchers have created many other kinds of

MLIs, However, 3-level MLIs suffer from both related and distinct restrictions. These traditional MLIs are fully utilized for demanding industrial tasks that require specific voltage output up to eight levels. They require a lot of devices to produce a higher-level voltage waveform. More diodes and DC link capacitors are needed for DC MLIs, more capacitors are needed for FC MLIs, and more DC power supplies are needed for CHB MLIs. Therefore, a few drawbacks of traditional MLIs, such as the need for additional A rise in the quantity, dimensions, and expense of inverters, as well as DC sources and switches, are eliminated [32]. This year, a number of researchers concentrated on topological advancement in MLI configuration to address the imbalance issue with capacitor voltage. In recent years, a number of MLIs with lower device counts have been proposed [33]. But these configurations aren't capable of self-boosting. because of intricate support algorithms, circuits like those in [33] have been suggested to lessen the unbalance issue in voltage of a capacitor. A 7-level topology is also provided in [34] with the benefit SC MLI based technique. In addition, [35] uses ten switches instead of twenty to produce a seven-level voltage output, reducing the total number of switches. Later on, a number of SC MLIs were revealed in published works. A greater number of switches, more capacitors, higher voltage stress, or low voltage gain are required for certain of them. It has inspired the creation of a brand-new, compact module structure.

An SCMLI's capacity to function at greater switching frequencies is another benefit. Higher voltage switching devices are not necessary as a result of the output voltage being generated using several levels, allowing for an increase in switching frequency. This raises overall efficiency and lowers switching losses [36]. Additionally, big inductors, which can be heavy and costly are not necessary due to the output voltage being produced by capacitors. A primary obstacle associated with SCMLI is the requirement for meticulous capacitor balance. It is crucial to ensure that the voltage of each capacitor is balanced because every inverter cell has a distinct requirement for a capacitor value [37]. Many balancing strategies, including voltage clamping and energy redistribution, can be used to accomplish this. In addition, the inverter needs to be precisely engineered to guarantee that the switching signals are synchronized. The design of a novel 7-level SC MLI is presented in this paper with only 10 switches and one DC supply. With this design, a single DC source can produce an output of a nine-time boosted staircase. Recently, a variety of switching strategies have emerged for MLI control [38]. Many methods are employed, including the selective distortion reduction pulse-width modulation (SHE PWM) in [39], the multi vector space technique in [38, 39], and [38] describes the use of several triangular carriers in the sinusoidal switching pulse technique.

The ability of the MLIs to provide stairway pattern output is their main advantage. The MLIs' primary benefit is their capacity to generate an output of staircase patterns. Hence, in contrast to three-level inverters, the output has less harmonic content. As a result, MLIs of various categories are highly common in photovoltaic (PV), FACTs, electric cars, and traction applications [40]. The modularity feature of conventional CHB MLI, which has many applications, is explored in both symmetrical and asymmetrical modes. Compared to symmetrical circuits, asymmetrical circuits generate more levels with fewer switches. Nonetheless, more switches and numerous DC sources are required. For this reason, it's critical to create a novel inverter construction using a single DC-bus and fewer components. Although structures provided by [41, 42] attempted to decrease the quantity of switches, a notable decrease was not accomplished. An extra charging circuit is integrated into the traditional arrangement in [40]. One benefit is that a single input source can raise the output voltage. A different circuit from the traditional CHB MLI was also altered in [41]. It is evident from the functioning that the Capacitors are filled and emptied as needed, which contributes to raising the resulting voltage. In particular, the solutions suggested in applications [43] are intriguing for PV applications. While one of the circuits utilizes a self-balancing capacitor based on energy regulating concept to cut down on the quantity of sources, the other MLI balances the voltage using the SC concept. The voltage can be significantly increased by the other MLI, while the former is unable to do so. In order to produce boost output voltage, newly proposed SC topologies take into account a reduction in both the quantity of parts and the stress on each switch [44, 45]. This construction can be used in various applications since it maintains the intrinsic voltage balancing of each capacitor while producing a high-gain output without the need for a large transformer or inductor. There are some circuit topologies described in [46] that require consideration for capacitor voltage balancing. using the fewest possible switches. Numerous other seven-level layouts have been proposed that take into account both single-stage and voltage boosting uses. More recently, topologies with NPC and common-neutral connections have been suggested to reduce the leakage current. While the later categories are added in [47], the former ones are recommended in [48], and they retain all other advantages.

The intricate control circuitry of SCMLI technology presents another difficulty. A sophisticated control circuit is needed for the inverter since the voltages of the capacitors and switching signals must be precisely controlled. Designing and implementing this can be difficult, especially for high-power applications. Despite these difficulties, there are a number of exciting uses for SCMLI technology. High-quality AC waveforms are necessary for renewable energy systems to interface with the grid, which is one possible application. Moreover, accurate output voltage regulation is essential for motor control, an area in which SCMLI technology finds use. Compared to conventional two-level

inverters, they have a number of advantages [49]. However, the technique is difficult to design and deploy since it requires intricate control circuitry and careful capacitor balancing. Notwithstanding these difficulties, SCMLI technology has a number of exciting uses, especially in motor control, alternative energy sources, and useful applications. Researchers are currently focusing on the switched capacitor multilayer as a result [50].

All things considered, the SHE PWM control method is excellent, low frequency of switching, controllable, and it eliminates output voltage harmonics. This study determines the output voltage and regulates the inverter's switching angles using the SHE PWM control approach. The suggested inverter is appropriate for applications involving sustainable and renewable energy sources were scaling up low input-side DC voltages is necessary. The recommended converter functionality is evaluated through simulation using the PSIM/MATLAB program.

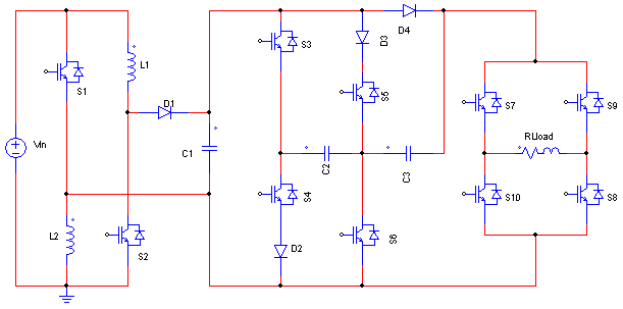


**Fig. 1. 7-Level SI/SC based seven level converters.**

## 1. OPERATION OF PROPOSED 7-L SC/SI MULTY LEVEL INVERTER

The suggested 7-Level SI/SC based multi-level inverter technology comprises 10 No. of power switches (namely S1 to S10), 2No. of inductors (namely L1 and L2), 3 No. of capacitors (namely C1, C2, and C3), and 4 No. of diodes (namely D1, D2, D3, and D4). The input voltage source Vin serves as the inverter's input, and Vo serves as its output voltage. The figure 1 shows single DC source 7-L SC/SI MLI, a multilayer inverter based on SI and SC, operates in single phase. This circuit has advantages of identical pulse triggering for the different switches. Switches S1 & S2 are triggered identically. And switches S7 and S8 triggered at a time. And also Switches S4, S9 triggered along with S5, S10.

### *2.1. Operating modes of 7-Level SI/SC based MLI*

The voltage produced by a staircase wave with seven levels is produced using ten switches and two capacitors. At the resultant voltage waveform, there are 3 no. of positive and 3 no. of negative levels and 01 no. of zero level make up the seven levels. ±3Vin, ±6Vin, ±9Vin, and 0 are produced by the structure using input voltage source Vin. The operational analysis is provided, taking into consideration the inductive load and the fact that all of the switches are made of antiparallel diodes. The following thirteen operating modes are available to generate the seven levels of the output waveform:

*1) Mode I (Level_1 ($3V_{in}$), high frequency power switches S1 and S2 are kept off)*

Switches S1 to S5, S9, and S10 produce an output level of +3Vin in this operating mode which are in turn off mode and S6 to S8 are in in turn on mode. Diode D1 and D4 is in forward conduction, D2 and D3 are reverse blocking mode, the capacitors C1 and C3 are charged by input power source Vin, inductors L1 and L2. The energy that inductors stored is at a level of input voltage. capacitor C2 is in ideal mode. the output level +3Vin is achieved by Vin, VL1 and VL2. the direction of charging/discharging currents are shown in figure 2.

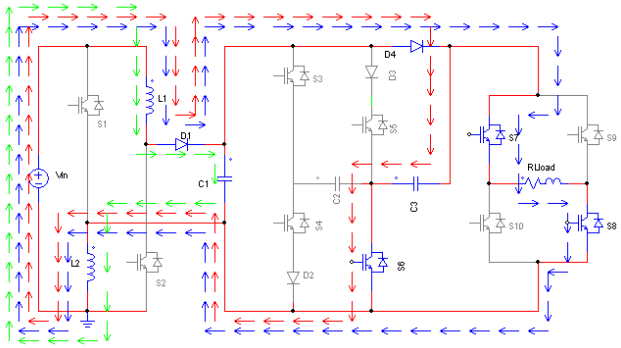


**Fig. 2. Mode I (Level_1) Direction of charging and discharging currents.**

*2) Mode II (Level_1 ($3V_{in}$), high frequency power switches S1 and S2 are kept on)*

In this mode, the output level +3Vin is obtained when switches S3 to S5, S9, and S10 are in turn off mode, S1, S2, S6, S7, and S8 are in in turn on mode. Diode D4 is in forward conduction mode, D1, D2 and D3 are reverse blocking mode, the capacitors C1 and C3 will supply its stored energy at a level of +3Vin to the load. The input voltage source Vin is going to power both inductors L1 and L2. the direction of both recharging/draining currents are shown in figure 3.

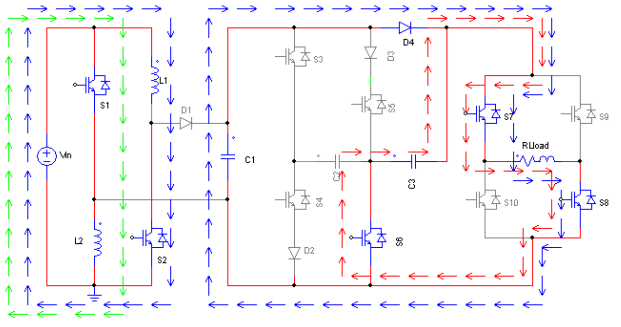


**Fig. 3. Mode II (Level_1) Direction of charging and discharging currents.**

*3) Mode III (Level_2 (6Vin), high frequency power switches S1 and S2 are kept off).*

When switches S1 to S3, S6, S9, and S10 are in turn off mode and switches S4, S5, S7, and S8 are in turn on mode, the level two output voltage +6Vin is obtained in this operating mode. Diode D1, D2 and D3 is in forward conduction, D4 is reverse blocking mode, The input voltage source Vin energizes the capacitors C1 as well as C2, inductors L1 and L2. The energy that inductors store is at a level of input voltage. capacitor C3 is in discharging mode its voltage is at a level of 3Vin which is charge in mode II. the output voltage +6Vin is achieved by series combination of Vin, VL1, VL2 and VC3. Figure 4 displays the charging /discharging current directions.

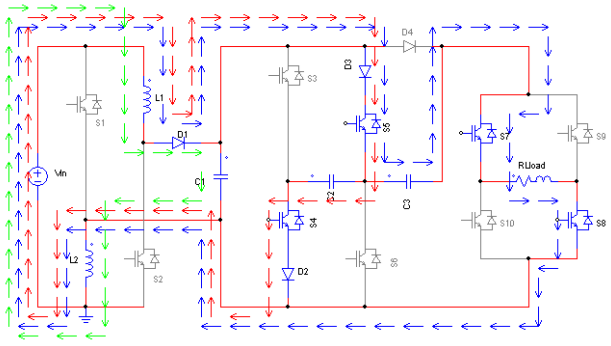


**Fig. 4. Mode III (Level_2) Direction of charging and discharging currents.**

*4) Mode IV (Level_2 (6Vin), high frequency power switches S1 and S2 are kept on).*

In this mode, the output level +6Vin is obtained when switches S3, S6, S9, and S10 are in turn off mode, S1-S2, S4-S5, S7-S8 are in in turn on mode. Diode D1 and D4 is in reverse biased mode, D2 and D3 are in forward conduction mode, the C1, C2 and C3 will supply the stored energy at a level of +6Vin to the load. Capacitors all are at a voltage level of +3Vin but capacitors C1 and C2 are in parallel and C3 is in series with the combination. The input voltage source Vin will charge both L1 and L2. the direction of charging/discharging currents are shown in figure 5.

*5) Mode V (Level_3 (9Vin), high frequency power switches S1 and S2 are kept off).*

When switches S1-S2, S4-S6, S9-S10 are in turn off mode and switches S3, S7, and S8 are in turn on mode, the level three output voltage +9Vin is reached in this working mode. Diode D1 is in forward conduction mode, diodes D2, D3, and D4 are in reverse blocking mode, the capacitors C1 is charged by its input source Vin, L1 and L2. The energy that inductors stored is at a level of input voltage. C2 and C3 is in discharging mode its voltage is at a level of 3Vin which is charge in mode III and Mode II. the output voltage +9Vin is achieved by the series combination of Vin, VL1, VL2, VC2 and VC3. Figure 6 displays the charging/discharging current directions.

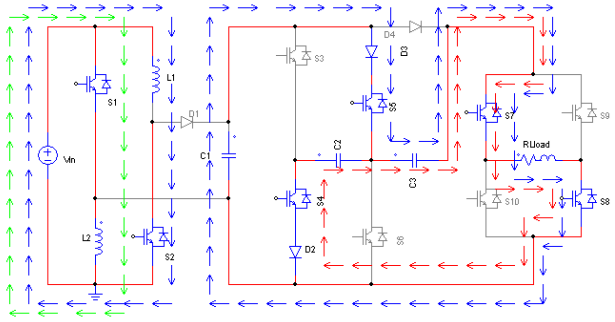


**Fig. 5. Mode IV (Level_2) Direction of charging and discharging currents.**

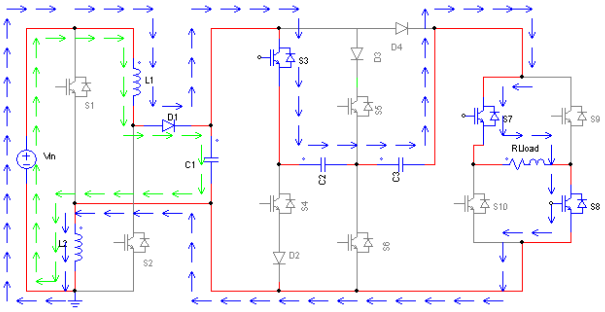


**Fig. 6. Mode V (Level_3) Direction of charging and discharging currents.**

*6) Mode VI (Level_3 (9Vin), high frequency power switches S1 and S2 are kept on).*

In this mode, the level three output voltage +9Vin is obtained when switches S4-S6, S9-S10 are in turn off mode, S1-S3, S7-S8 are in in turn on mode. Diode D1-D4 is in reverse biased mode, the capacitors C1-C3 will supply the stored energy at a level of +9Vin to the load. Capacitors all are at a voltage level of +3Vin which is stored in previous modes but capacitors C1-C3 are in series. Vin will charge the inductors L1 and L2. Figure 7 displays the charging/ discharging current directions.

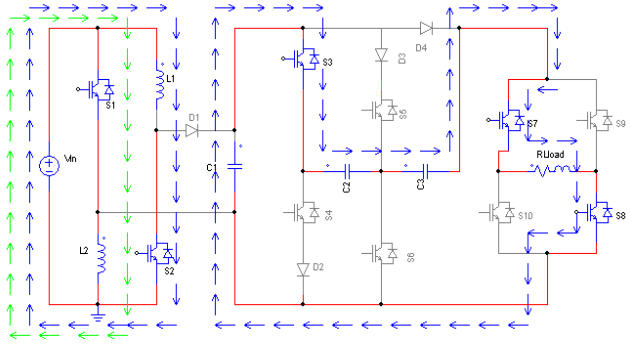


**Fig. 7. Mode VI (Level_3) Direction of charging and discharging currents.**

*7) Mode VII (Level_1 (-3Vin), high frequency power switches S1 and S2 are kept off).*

This mode is identical to the mode I, but the status of the switches S7-S9, S10 are changed. During this operating mode, the output level -3Vin is achieved when switches S1-S5, S7-S8 are in turn off mode and S6, S9, and S10 are in in turn on mode. Diode D1 and D4 is in forward conduction, D2 and D3 are reverse blocking mode, Condensers C1 and C3 are charged by Vin, L1 and L2. The stored energy in Inductors is at a level of input voltage. capacitor C2 is in ideal mode. the output level -3Vin is achieved by the series combination of Vin, VL1 and VL2. Figure 8 displays the charging/discharging current directions.

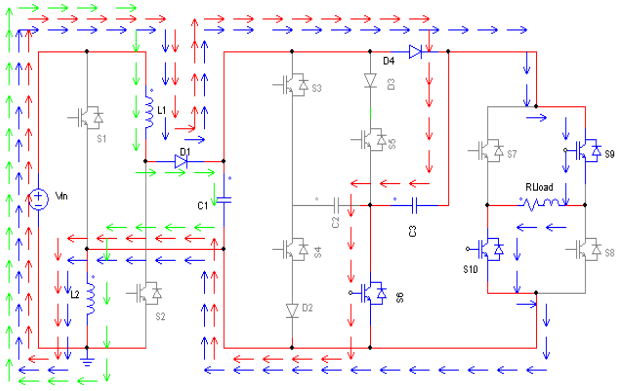


**Fig. 8. Mode VII (Level-1) Direction of charging and discharging currents.**

*8) Mode VIII (Level_1 (-3Vin), high frequency power switches S1 and S2 are kept on)*

This mode is identical to the mode II, but the status of the switches S7, S8, S9, S10 are changed. In this mode, the output level -3Vin is obtained when power switches S3-S5, S7-S8 are in turn off mode, S1, S2, S6, S9, and S10 are in in turn on mode. Diode D4 is in forward conduction mode, D1, D2 and D3 are reverse blocking mode, the capacitors C1 and C3 will supply the stored energy at a level of -3Vin to the load. The Vin will charge both inductors L1 and L2. Figure 9 displays the charging/ discharging current directions.

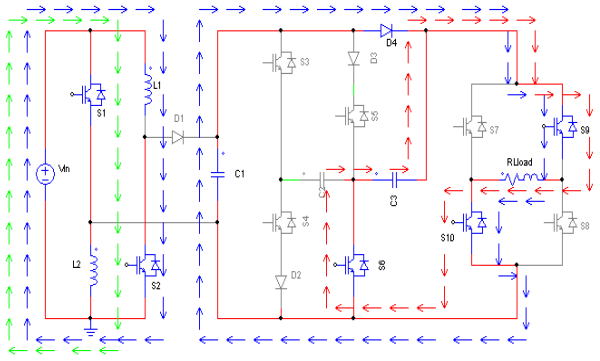


**Fig. 9. Mode VIII (Level_1) Direction of charging and discharging currents.**

*9) Mode IX (Level_2 (-6Vin), high frequency power switches S1 and S2 are kept off).*

This mode is identical to the mode III, but the status of the switches S7-S10 is changed, in this operating mode, the output level -6Vin is obtained when switches S1, S2, S3, S6, S7, and S8 are in turn off mode and S4, S5, S9, and S10 are in in turn on mode. Diode D1-D3 is in forward conduction, D4 is reverse biased mode, The source voltage Vin charges both capacitors C1 and C2. and L1 and L2. The stored energy in Inductors is at a level of input voltage. capacitor C3 is in discharging mode its voltage is at a level of 3Vin which is charge in mode II. the output voltage -6Vin is get by the series combination of Vin, VL1, VL2 and VC3. Figure 10 displays the charging/discharging current directions.

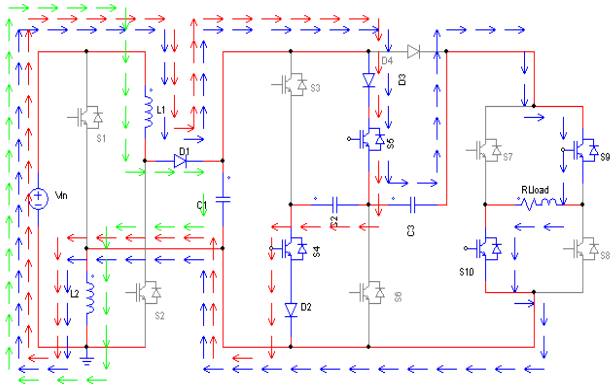


**Fig. 10. Mode IX (Level_2) Direction of charging and discharging currents.**

*10) Mode X (Level_2 (-6Vin), high frequency power switches S1 and S2 are kept on).*

This mode is identical to the mode IV, but the status of the switches S7, S8, S9, S10 are changed. In this mode, the output level -6Vin is obtained when switches S3, S6, S7, and S8 are in turn off mode, S1, S2, S4, S5, S9, and S10 are in in turn on mode. Diode D1 and D4 is in reverse biased mode, D2 and D3 are in forward conduction mode, the capacitors C1, C2 and C3 will supply the stored energy at a level of -6Vin to the load. Capacitors all are at a voltage level of -3Vin but capacitors C1 and C2 are in parallel and C3 is in series with the combination. both inductors L1 and L2 will be charged by the input voltage source Vin. Figure 11 displays the charging/discharging current directions.

*11) Mode XI (Level_3 (-9Vin), high frequency power switches S1 and S2 are kept off).*

This mode is identical to the mode V, but the status of the switches S7-S10 is changed. In this operating mode, the output level -9Vin is obtained when switches S1, S2, S4, S5, S6, S7, and S8 are in turn off mode and S3, S9, and S10 are in turn on mode. Diode D1 is in forward conduction mode, diodes D2-D3, and D4 are in reverse blocking mode, the

capacitors C1 is charged by Vin, inductors L1 and L2. The stored energy in Inductors is at a level of input voltage. Capacitors C2 and C3 is in discharging mode its voltage is at a level of 3Vin which is charge in mode III and Mode II. the output voltage -9Vin is obtained by the series combination of Vin, VL1, VL2, VC2 and VC3. Figure 12 displays the charging/discharging current directions.

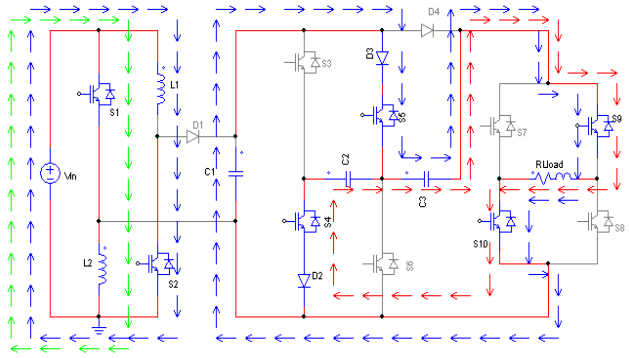


**Fig. 11. Mode X (Level_2) Direction of charging and discharging currents.**

*12) Mode XII (Level_3 (-9Vin), high frequency power switches S1 and S2 are kept on)*

This mode is identical to the mode VI, but the status of the switches S7, S8, S9, S10 are changed. In this mode, the output level -9Vin is achieved when switches S4-S8 are in turn off mode, S1, S2, S3, S9, and S10 are in in turn on mode. Diode D1-D4 is in reverse biased mode, the capacitors C1- C3 will supply the stored energy at a level of -9Vin to the load. Capacitors all are at a voltage level of -3Vin which is stored in previous modes but capacitors C1, C2 and C3 are in series. both inductors L1 and L2 are magnetized by the input voltage source Vin. Figure 13 displays the charging /discharging current directions.

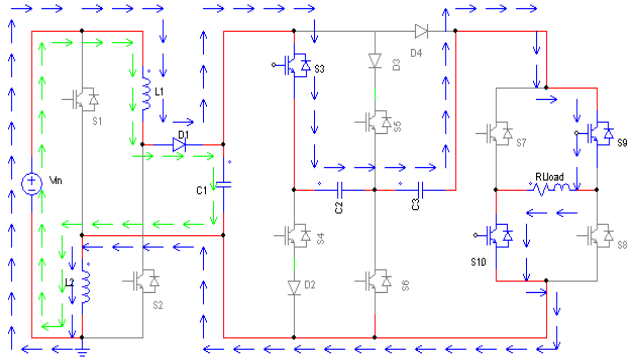


**Fig. 12. Mode XI (Level_3) Direction of charging and discharging currents.**

*13) Mode XIII (Level_0 (0Vin)*

In this configuration, the two remaining S7 and S9, are in conduction mode and switches S1, S2, S3, S4, S5, S6, S8, and S10 are in the off position. The zero-level output can be produced by activating either two lower switches or two top switches connected to the bridge circuit. table 1 displays the switching scheme of the 7-L SC/SI MLI with seven distinct voltage levels (+Vdc, -Vdc, +2Vdc, -2Vdc, +3Vdc, -3Vdc, and 0Vdc) as well as the capacitors and inductors charging and discharging times.

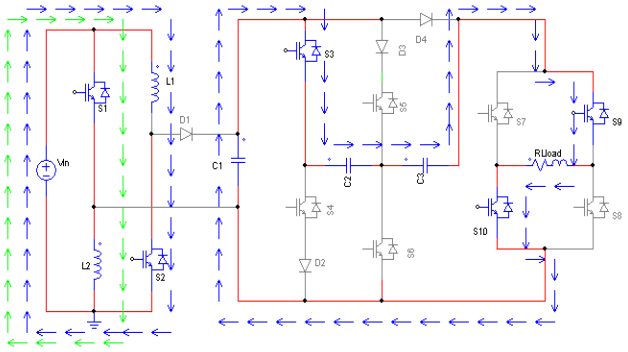


**Fig. 13. Mode XII (Level_3) Direction of charging and discharging currents**

### *2.2. Voltage Self-balancing Analysis*

It is evident based on the functional analysis covered in Section 2.1, whereby the capacitor C1 gets charged both when the power is switched on and off. Capacitor C2 discharged in the remaining states after being charged between +6 and -6 volts. Conversely, the capacitor C3 experiences charging at Vdc and −Vdc, and discharging at 6Vin and -6Vin. As a result, the recharging and draining process is balanced. Additionally, the capacitors are discharged to the source to the load and charged in parallel with the DC source. Notable features include the minimal parasitic resistance and sufficient charging and discharging time for each capacitor in a single basic cycle. As a result, during the operation of the circuit, the voltage across Naturally, the capacitor is kept at Vin. this confirms the self-balancing nature, and the right capacitance is selected with the least amount of voltage ripple possible while accounting for the greatest time to discharge:

$$C_n \geq L_1 \frac{\Delta Q_c}{\Delta V_c} \quad = \frac{2I_{op}Cos(\theta_n)\cos(\Phi)}{k\psi V_{dc}} \qquad (1)$$

where, $\Delta V_c$, k (7-8%), and $\Delta Q_c$ are the capacitor's ripple voltage and percentage ripple, respectively, and the capacitor's amount of discharge rate. The variables $C_n$, $I_{op}$, the maximal load current flowing through the capacitors. $\theta_n$ is the power factor angle.

**Table 1. 7-Level SI/SC MLI's switching states along with the periods for capacitor/Inductor charging/discharging status**

| Voltage Level | Conducting switches | Inductor L1 and L2 | Capacitor C1 | Capacitor C2 | Capacitor C3 |
|---|---|---|---|---|---|
| O | S7, S9 | - | - | - | - |
| | S8, S10 | - | - | - | - |
| +3Vin | S6- S8 | ↓ | ↑ | - | ↑ |
| | S1-S2, S6-S8 | ↑ | ↓ | - | ↓ |
| +6Vin | S4-S5, S7-S8 | ↓ | ↑ | ↑ | ↓ |
| | S1-S2, S4-S5, S7-S8 | ↑ | ↓ | ↓ | ↓ |
| +9Vin | S3, S7-S8 | ↓ | ↑ | ↓ | ↓ |
| | S1-S3, S7, S8 | ↑ | ↓ | ↓ | ↓ |
| -3Vin | S6, S9-S10 | ↓ | ↑ | - | ↑ |
| | S1-S2, S6, S9-S10 | ↑ | ↓ | - | ↓ |
| -6Vin | S4-S5, S9-S10 | ↓ | ↑ | ↑ | ↓ |
| | S1-S2, S4-S5, S9-S10 | ↑ | ↓ | ↓ | ↓ |
| -9Vin | S3, S9-S10 | ↓ | ↑ | ↓ | ↓ |
| | S1-S3, S9-S10 | ↑ | ↓ | ↓ | ↓ |

## 2. COMPARATIVE ESTIMATION

A comparison with a few chosen topologies has shown the developed boost inverter topology's comparison capabilities. Table 2 shows a contrast between the recommended 7-level 9 times voltage gain boost inverter design and some of the other topologies that have been proposed previously. The number of 'switches, diodes, inductors, capacitors, input sources, gate drivers, gains' in the topology, and whether or not polarity is created intrinsically are the factors that are compared. In [51], the architecture uses more gate drivers and an additional capacitor but has one fewer switch than the recommended topology. The recommended topology is lower than the 'Maximum Blocking Voltage (MBV)' on switches and The 'Total Standing Voltage (TSV)'. There is the same quantity of components overall in [52]'s topology, but it has a low voltage gain of three and a large TSV. the topology in [53-54] has a larger MBV and a larger voltage rating capacitor. The topology in [55] is more extensive in terms of switches used and has a higher TSV value than the suggested topology. In contrast to the recommended topology, H-bridge is used in Reference [56] to generate polarity, which results in high TSV and MBV values.

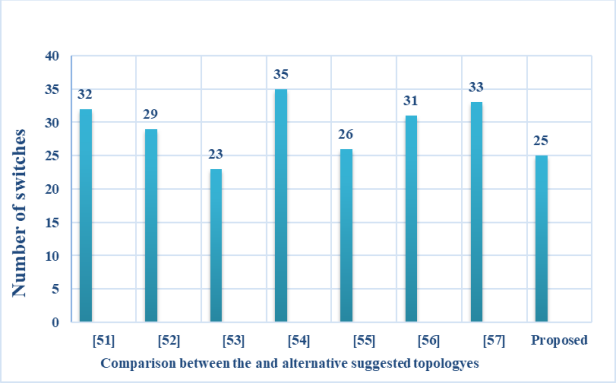


**Fig. 14. Comparison of suggested configuration based on the quantity of switches.**

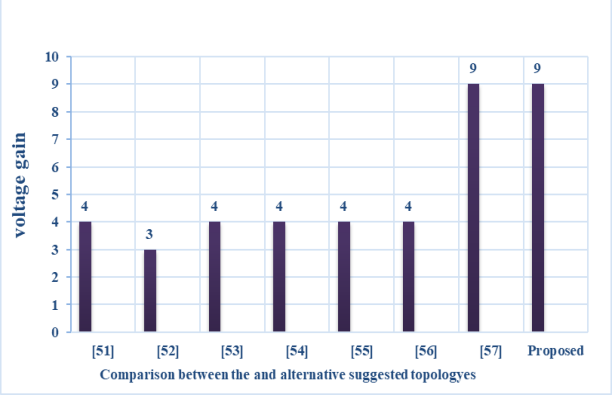


**Fig. 15. comparison of suggested configuration based on the voltage gain.**

The recommended generalized topology and many rival generalized topologies are contrasted in Table 2. that have been proposed recently. The suggested design has lower TSV and MBV than the other topologies in Table 2, indicating that the switches are under less voltage stress. Its total number of components is equal to or less than that of the other items in Table 2. Comparing the topology with other topologies shown in the following table, there are more capacitors and diodes in it. the topology presented in [57] has high gain but a greater number of components. Figure 14, comparison of suggested configuration based on the quantity of switches and Figure 15, comparison of suggested configuration based on the voltage-gain.

Table 2 compares the suggested generalized topology with other competing generalized topologies. that have just been put forth. Compared to the alternative topologies in Table 2, the recommended design has lower TSV and MBV, suggesting that the switches are under less voltage stress. Its overall component count is either the same as or lower than that of the other items in Table 2. The topology shown here has more capacitors and diodes than the other topologies shown in the table below. The topology described in [57] has more components but a high gain. Figures 14 and 15 compare the recommended configurations according to the no. of switches and voltage-gain, respectively.

The suggested seven-level inverter architecture and recently published seven-level converter structures from the literature are thoroughly contrasted in Table 2. The no. of power switches, inductors, capacitors, diodes, gate driver circuits, voltage gain, maximum blocking voltage, H-bridge required, and overall component count are among the key performance and design factors that form the basis of the comparison.

The comparison shows that traditional topologies described in [51-56] often produce a voltage gain between 3 and 4, which restricts their applicability for low-voltage solar applications where significant step-up capability is crucial. The suggested converter, on the other hand, obtains a much larger voltage gain of 9, which makes it ideal for renewable energy systems that use low DC input voltage sources.

Topology [57] also offers a voltage gain of 9, but it uses a lot of semiconductor and passive parts, such as 12 diodes and 5 capacitors, which raises the implementation cost, conduction losses, circuit complexity, and control difficulty. By using just three capacitors and four diodes, the suggested design avoids these problems while preserving the same high voltage gain.

The proposed converter also demonstrates reduced hardware complexity by requiring only 10 switches and 6 gate driver circuits. A lower number of gate drivers simplifies the control architecture and reduces isolation requirements, gate-driving losses, and overall controller cost. This feature is particularly advantageous in compact and cost-sensitive PV power conversion systems.

The proposed converter also demonstrates reduced hardware complexity by requiring only 10 switches and 6 gate driver circuits. A lower number of gate drivers simplifies the control architecture and reduces isolation requirements, gate-driving losses, and overall controller cost. This feature is particularly advantageous in compact and cost-sensitive PV power conversion systems.

The lower maximum blocking voltage across the switches is another important benefit of the suggested topology. While many current topologies show blocking voltages of four or more, the maximum blocking voltage per unit is restricted to three. Utilizing lower-rated semiconductor devices is made possible by lower voltage stress, which raises converter reliability, decreases switching losses, and increases efficiency.

**Table 2. The suggested topology is contrasted with alternative seven-level topologies**

| Converter proposed in | No. of switches | No. of inductors | No. of capacitors | No. of diodes | No. of gate drivers | Voltage gain | Maximum blocking voltage | H-bridge | Total no. of components |
|---|---|---|---|---|---|---|---|---|---|
| [51] | 14 | 0 | 4 | 0 | 14 | 4 | 4 | No | 32 |
| [52] | 12 | 0 | 4 | 2 | 11 | 3 | 3 | Yes | 29 |
| [53] | 10 | 0 | 2 | 1 | 10 | 4 | 4 | No | 23 |
| [54] | 16 | 0 | 3 | 0 | 16 | 4 | 4 | No | 35 |
| [55] | 10 | 0 | 3 | 3 | 10 | 4 | 4 | Yes | 26 |
| [56] | 15 | 0 | 3 | 0 | 13 | 4 | 3 | No | 31 |
| [57] | 8 | 2 | 5 | 12 | 6 | 9 | 9 | Yes | 33 |
| Proposed | 10 | 2 | 3 | 4 | 6 | 9 | 3 | Yes | 25 |

Furthermore, in order to provide both positive/negative output voltage levels, a number of traditional topologies need an external H-bridge stage. The no. of switches, gate driver needs, and overall circuit size all rise when an H-bridge is added. The suggested converter reduces complexity and increases power density by doing away with the requirement for an extra H-bridge while still producing a seven-level voltage.

With the exception of [53], the proposed converter uses fewer components overall just 25 than the majority of documented topologies. Nevertheless, topology [53] lacks the significant boosting capability attained by the suggested converter and only offers a voltage gain of 4. As a result, the suggested design provides a better trade-off between voltage boosting performance and component count.

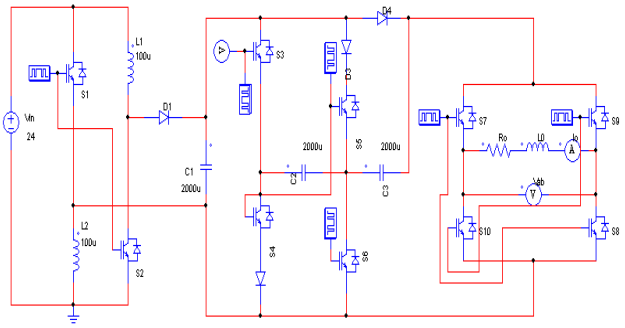

**Fig. 16. Simulation circuit of proposed inverter.**

## 3. SIMULATION RESULTS

IGBT switches, inductors, capacitors, and diodes make up the 7-LevelSI/SC MLI, as depicted in Figure 16, and they are all simulated using the PSIM/MATLAB/Simulink platform. The simulation uses Vin 24V, inductors L1, L2 are rated at 100uh, and C1, C2, and C3 are rated at 2000uf. Figure.17(a-e) displays the output AC power supply voltage with 24V input DC voltage, output load current, capacitors C1, C2 and C3 balanced voltages of the suggested design under an RL load of 100 ohm - 120 mH. Three balanced capacitor voltages and seven stages of output voltage with a peak amplitude of 216V are present. The suggested MLI's dynamic operational capability is shown in Fig. 18. Fig. 18(a) illustrates how the load current gradually transitions from being solely resistive to sinusoidal-like with inductive loading when the load suddenly changes. The results confirm that there are also very little ripples in the the capacitor voltage. The smooth transition between the output and capacitor voltages caused by the abrupt shift in input voltage is shown in Figure 18(b). Under any scenario of operation, the capacitor voltages have been adjusted to the proper value.

During the capacitor charging process, large current spikes, also known as inrush current, are an inevitable serious problem in SC circuits. The issue is raised in every SC MLI that has been released thus far. However, a recently designed structure in [51] overcomes the problem of capacitor current by using a quasi-resonant cell in the input side. The quasi-resonant cell restricts the inrush current of the capacitor during charging by choosing the appropriate values for the tiny inductor and capacitor ($L_{in}$ and $C_{in}$). Although the current spikes cannot be totally eliminated by the suggested topology as described in the article, by joining the quasi-resonant cell as in [52], they can be reduced. When considering the charging loop utilizing the equivalent capacitance (Ceq), the equivalent series resistance (Req) is taken into account. when choosing the resonant cell inductance, as follows:

$$L_{in} \geq \frac{R_{eq}{}^2 C_{eq}}{4} \quad (2)$$

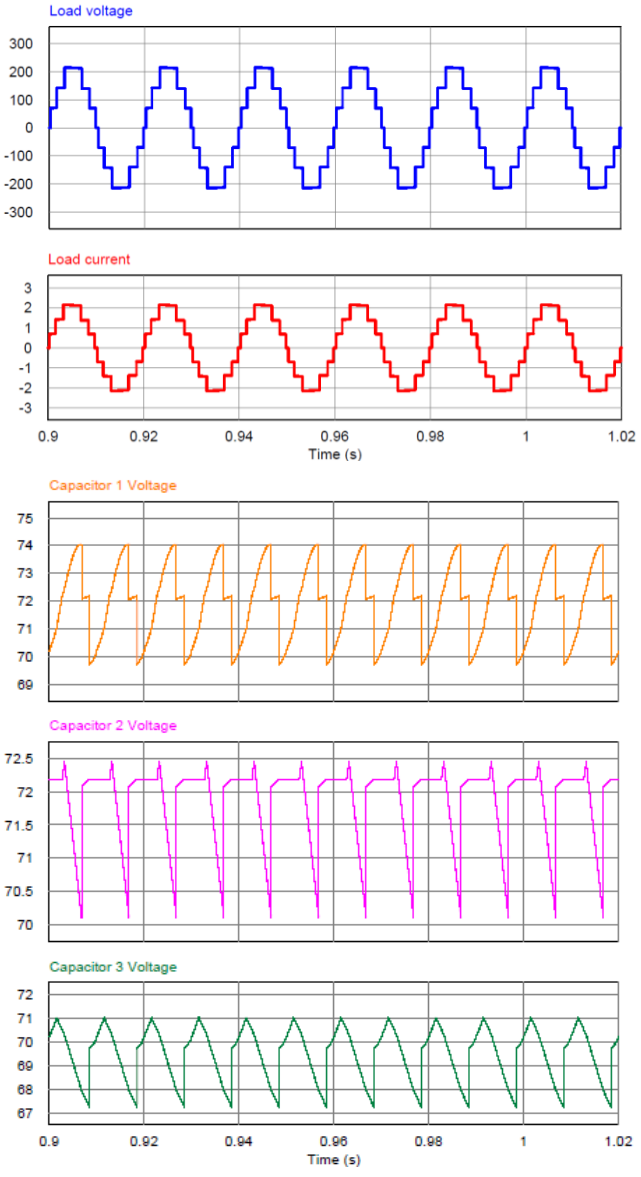


**Fig. 17(a). Load voltage (b) Load current (c-e) voltage balancing of capacitor C1, C2 and C3 .**

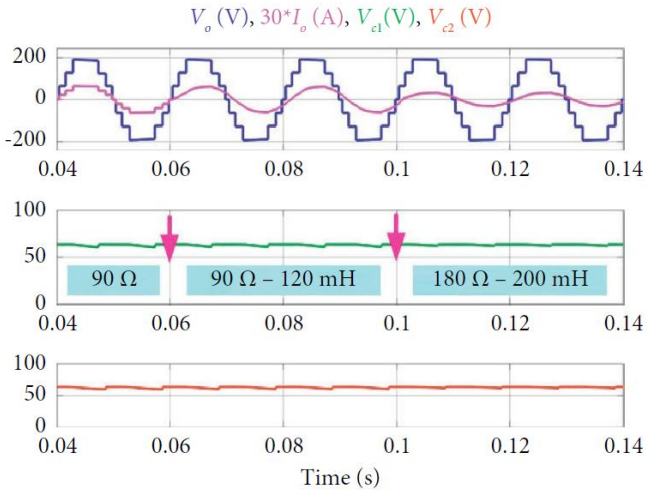


**Fig. 18(a). Dynamic functioning of the suggested MLI outcome during abrupt changes in loading.**

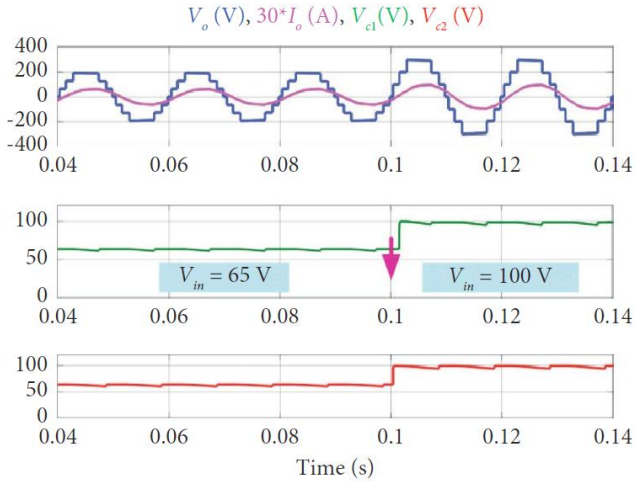


**Fig. 18(b). The suggested MLI operates dynamically in response to abrupt changes in input voltage.**

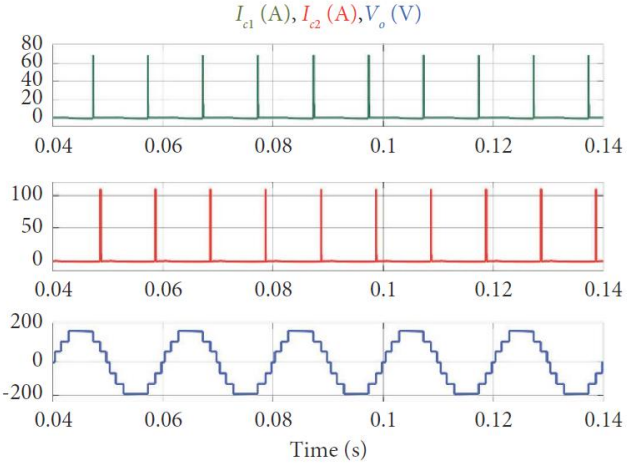


**Fig. 18(c). Dynamic functioning of the suggested MLI capacitor currents in the absence of a resonant cell.**

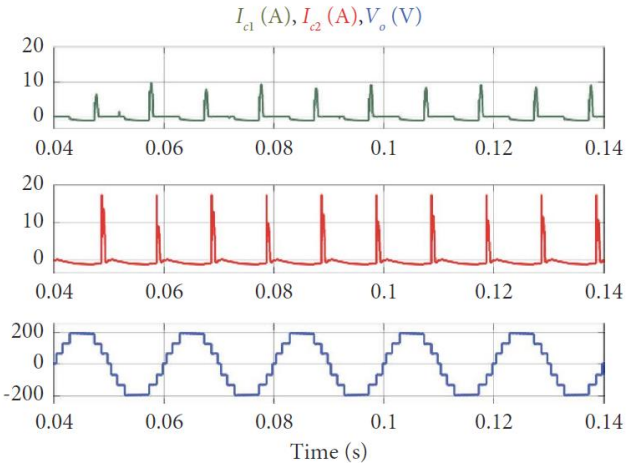


**Fig. 18(d). Using the resonant cell, the suggested MLI capacitor currents operate dynamically.**

The capacitor currents as well as output voltage are depicted in Figures 18(c) and 18(d), respectively, both without and with the quasi-resonant cell used. Even after accounting for the charging path's parasitic resistance, it is evident that the charging currents of the SC type MLIs during normal operation are rather large (50 times). The capacitor current is significantly decreased while maintaining the MLI's 7-L functionality when the resonant cell is taken into consideration.

## 4. CONCLUSION

For small-scale photovoltaic applications, this research suggests nine times boost seven-level inverter and a high gain generalized MLI. Low stress across the switches and capacitor self-balancing voltage are its benefits. A comparison analysis is carried out with current literature. The suggested architecture is appropriate for all types of loads and has been tested under various load, supply voltage, and frequency fluctuations. Additionally, the capacitor's voltage ripples stay within permitted bounds with various load fluctuations. A high-gain nine-times boost seven-level inverter topology appropriate for small-scale solar applications is shown in this paper. Reduced voltage stress on switches and intrinsic capacitor voltage self-balancing capability are two benefits of the suggested generalized multilayer inverter (MLI). The suggested configuration's performance has been assessed and contrasted with other topologies that have been documented in the literature. The designed architecture exhibits resilience and dependability as it functions well under various load situations, input voltage variations, and frequency changes. Furthermore, even when the load fluctuates dynamically, the capacitor voltage ripple stays within reasonable bounds. The suggested 7-level switched-capacitor (SC) MLI reduces circuit complexity and expense by using a single DC source and fewer power switches. Without the need for extra balancing circuits, the output voltage gain reaches three

times the input voltage amplitude due to the capacitors' self-balancing characteristic. It is also possible to optimize the capacitor sizing for high-frequency operation. Several current MLI topologies have been thoroughly compared, taking into account variables like component count, TSV, voltage boosting capability, and functioning under various load situations. The comparison validates the suggested inverter structure's enhanced performance and appropriateness. Additionally, minimal switching losses and better output waveform quality at the fundamental frequency are guaranteed when the SHE-PWM technique is used. The efficiency of the suggested topology in generating a high-gain seven-level output under varied operating situations is confirmed by simulation and experimental studies. For low- and medium-power converting energy applications, especially in renewable energy systems, the suggested inverter might thus be regarded as a promising solution. Results from simulations and experiments confirm that divergent operating modes are suitable for generating high-gain 7-level output. There are numerous uses for the proposed architecture in low- and medium-power energy conversion.

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