A Hybrid PWM Method for Capacitor Voltage Balancing in Four-Level π-Type Inverters

Duc Dung Le[1], Thanh Toi Le[1,*], and Duc Anh Tuan Nguyen[1]

ARTICLE INFO

Article history:
Received: 6 October 2024
Revised: 9 February 2025
Accepted: 10 March 2025
Online: 20 July 2026

Keywords:
Hybrid PWM
Four-level π-type
Voltage balancing
Power losses reduction

ABSTRACT

This paper proposes a novel hybrid pulse-width modulation (PWM) technique for the four-level π-type inverter. The proposed PWM scheme combines carrier-overlapped (CO) PWM and conventional level-shifted (LS) PWM to optimize performance across various modulation index ranges. In the low modulation range, LSPWM is applied together with a zero-sequence-voltage-based scheme to maintain capacitor voltage balance. For modulation indices above 0.5, the COPWM scheme is adopted to achieve automatic voltage balancing under ideal conditions. This hybrid approach effectively maintains the DC-link capacitors at their rated voltages under all operating conditions, thereby eliminating the need for any auxiliary balancing circuits in systems that use a passive front-end rectifier. In addition, it achieves lower switching losses and reduced total harmonic distortion (THD) compared to using COPWM alone, particularly at low modulation index ranges. The feasibility of this modulation technique and voltage control strategy is validated through simulation results from a 3 kVA inverter prototype.

1. INTRODUCTION

Due to its ability to enhance power density and quality, reduce electromagnetic interference, and support a wide range of DC input voltages, multilevel inverters (MLIs) have gained interest in low-power applications [1]-[8]. However, MLIs employing increased voltage levels, including four-level (4L) and five-level (5L) structures, require more power semiconductors and passive components, complicating both the circuit and control systems. The 4L π-type inverter reported in [9] offers advantages over conventional multilevel inverters, such as reduced complexity, fewer components, and lower conduction losses. As shown in Fig. 1, the topology requires only six power switches in each phase leg, eliminating the need for clamping diodes and flying capacitors, making it ideal for high-power density applications requiring. However, unequal DC-link capacitor voltages due to the multiple clamping points in the DC-link, as commonly observed in NPC-type converters, remains a key challenge for the 4L π-type topology [9], [10].

Various capacitor-voltage balancing strategies have been reported, which are generally classified into two categories: software-based and hardware-based methods [11], [12]. In software-based approaches, a zero-sequence voltage (ZSV) component can be injected into the reference voltage signals under the level-shifted PWM (LSPWM) modulation method to balance the DC-link capacitor voltages [13], [14].

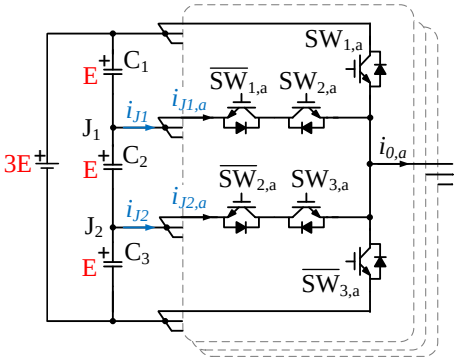


Fig. 1. Circuit diagram of there-phase 4L π-Type inverter.

Similarly, when using the nearest-three-vectors (NTV) approach for space-vector modulation (SVM), the capacitor voltages can be balanced within specific operating ranges [15]. However, these methods are ineffective when the inverter operates in higher modulation index regions, as defined by the theoretical boundaries in [15]. Hardware-based solutions can bypass theoretical limitations and enhance capacitor voltage balancing by a back-to-back converter configuration [16], or incorporating extra balancing circuits [17], [18]. However, these approaches need extra hardware, leading to higher system cost and complexity.

[1]*Department of Electrical and Electronic Engineering, Ho Chi Minh city University of Industry and Trade, Ho Chi Minh city, 760310, Vietnam.*
**Corresponding author:* Thanh Toi Le; Phone: +84-908-361-564; Email: toilt@huit.edu.vn.

Table 1. Switching-state combinations and output voltage levels of the 4L π-type inverter.

SW_1	SW_2	SW_3	Voltage states	v_{xN}	$i_{J1,x}$	$i_{J2,x}$
1	1	1	V_3	3E	-	-
0	1	1	V_2	2E	$i_{0,x}$	-
0	0	1	V_1	E	-	$i_{0,x}$
0	0	0	V_0	0	-	-

The carrier-overlapped (CO) PWM method, initially proposed for NPC-type converters, was introduced in [19] and further discussed in [20]. By overlaying multiple carrier signals, this PWM method generates more voltage levels within a single sample period. It also has the ability to preserve capacitor voltage balancing over the full operating range without requiring auxiliary balancing circuits. However, the main shortcomings of the COPWM are an increase in switching frequency, higher total harmonic distortion (THD), and significant switching losses, especially in the low modulation-index region.

To address the limitations of the COPWM approach, this research proposes a hybrid PWM strategy. It integrates LSPWM for modulation indices below 0.5 and COPWM for higher indices. Additionally, voltage balancing controls are developed for each PWM technique. This hybrid approach keeps all capacitor voltages balanced across the entire modulation-index range while reducing switching-related power losses at low modulation indices.

The rest of this paper is structured as follows. Section 2 discusses the capacitor-voltage balancing strategy for the LSPWM and COPWM schemes, respectively. Section 3 presents the PSIM simulation results for different operating scenarios. Finally, section 4 provides the conclusions.

2. HYBRID PWM MODULATION FOR BALANCING CAPACITOR VOLTAGES

2.1 DC-Link Capacitor Voltages Deviation

Table 1 shows that when the voltage level is 2*E*, the load current passes through NP J_1, and when it is *E*, it passes through J_2. Hence, the mean value of the single-phase junction currents is labeled as $I_{J1,x}$ and $I_{J2,x}$ in a sampling period T_{sp}, can be calculated as follows:

$$\begin{cases} I_{J1,x} = (d_{x2} - d_{x1}) \cdot i_{0,x} \\ I_{J2,x} = (d_{x3} - d_{x2}) \cdot i_{0,x} \end{cases} \quad (1)$$

where, d_{x1}, d_{x2}, and d_{x3} are the duty cycles of $SW_{1,x}$, $SW_{2,x}$, and $SW_{3,x}$ respectively. The total junction current is the sum up the all-single-phase junction current, which can express as:

$$\begin{cases} I_{J1} = \sum_{x=a,b,c} I_{J1,x} \\ I_{J2} = \sum_{x=a,b,c} I_{J2,x} \end{cases} \quad (2)$$

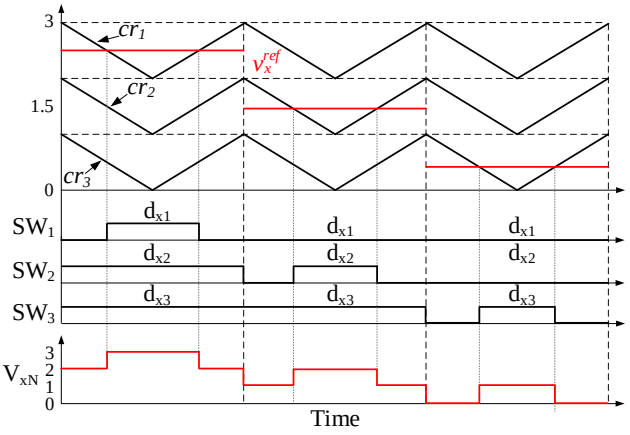


Fig. 2. Gating signals and output voltage of the 4L π-type inverter under LSPWM method.

The deviation of the DC-link capacitor voltage is caused by these total junction currents. The relationship between the DC-link capacitor voltages and the junction currents is expressed as follows:

$$\begin{cases} I_{J1} = I_{C1} - I_{C2} = C_{dc} \cdot d(v_{C1} - v_{C2}) / dt \\ I_{J2} = I_{C2} - I_{C3} = C_{dc} \cdot d(v_{C2} - v_{C3}) / dt \end{cases} \quad (3)$$

where, C_{dc} represents the capacitance of DC-link capacitors; v_{C1}, v_{C2}, and v_{C3} denote their corresponding capacitor voltages. From (3), under the assumption of a constant DC-link voltage, then the voltage mismatch among these capacitors in over one carrier period can be expressed as:

$$\Delta v_{C1} = (2I_{J1} + I_{J2}) \cdot T_{sp} / (3C_{dc}) \quad (4)$$

$$\Delta v_{C2} = (-I_{J1} + I_{J2}) \cdot T_{sp} / (3C_{dc}) \quad (5)$$

$$\Delta v_{C3} = (-I_{J1} - 2I_{J2}) \cdot T_{sp} / (3C_{dc}) \quad (6)$$

Equation (5) indicates that the middle DC-link capacitor experiences voltage imbalance according to the current difference between the upper and lower junction paths:

$$I_{J-} = -I_{J1} + I_{J2} = \sum_{x=a,b,c} \left[(d_{x1} - 2d_{x2} + d_{x3}) \cdot i_{0,x} \right] \quad (7)$$

The sum of two junction currents also can be formulated as,

$$I_{J+} = I_{J1} + I_{J2} = \sum_{x=a,b,c} \left[(-d_{x1} + d_{x3}) \cdot i_{0,x} \right] \quad (8)$$

Based on (4) and (6), the top-and-bottom capacitor voltage deviation is governed only by the combined junction current and can be expressed as

$$\Delta v_{C1-3} = \Delta v_{C1} - \Delta v_{C3} = I_{J+} \cdot T_{sp} / (C_{dc}) \quad (9)$$

This indicates that controlling the junction currents is the only viable approach to balancing all capacitor voltages in the DC-link. Furthermore, the junction currents depend on the PWM modulation method, as can be observed from (1) and (2). The voltage balancing methods for LSPWM and COPWM will be discussed in detail in the next section.

2.2. Voltage-Balancing Method Based on LSPWM

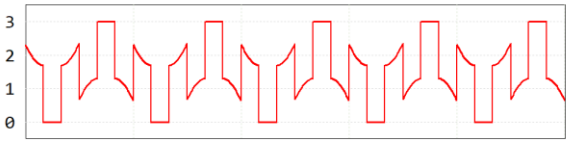
The LSPWM diagram for 4L π-type inverter is illustrated in Fig. 2. The duty cycles of $SW_{1,x}$, $SW_{2,x}$, and $SW_{3,x}$ are written as follows:

$$\begin{cases} d_{x1} = v_x^{ref} - 2; d_{x2} = 1; d_{x3} = 1 & \left[2 \le v_x^{ref} \le 3\right] \\ d_{x1} = 0; d_{x2} = v_x^{ref} - 1; d_{x3} = 1 & \left[1 \le v_x^{ref} < 2\right] \\ d_{x1} = 0; d_{x2} = 0; d_{x3} = v_x^{ref} & \left[0 \le v_x^{ref} < 1\right] \end{cases} \quad (10)$$

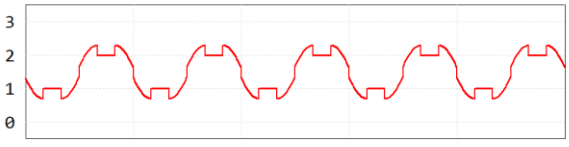
According to (8), the combined and differential junction currents within one sampling interval can be expressed as follows:

$$I_{j+} = \sum_{x=a,b,c} \begin{cases} \left(-v_x^{ref} + 3\right) \cdot i_{0,x} & \left[2 \le v_x^{ref} \le 3\right] \\ i_{0,x} & \left[1 \le v_x^{ref} < 2\right] \\ v_x^{ref} \cdot i_{0,x} & \left[0 \le v_x^{ref} < 1\right] \end{cases} \quad (11)$$

$$I_{j-} = \sum_{x=a,b,c} \begin{cases} \left(v_x^{ref} - 3\right) \cdot i_{0,x} & \left[2 \le v_x^{ref} \le 3\right] \\ \left(-2v_x^{ref} + 3\right) \cdot i_{0,x} & \left[1 \le v_x^{ref} < 2\right] \\ v_x^{ref} \cdot i_{0,x} & \left[0 \le v_x^{ref} < 1\right] \end{cases} \quad (12)$$



(a) Offset voltage with minimum I_{J-}



(b) Offset voltage with maximum I_{J-}

Fig. 3. Reference voltage after injecting ZSV.

The average value of I_{J+} is zero over a fundamental period, resulting in identical voltage profiles for the top and bottom capacitors, which increase or decrease simultaneously. The average value of I_{J-} is always positive if no balancing control is applied, leading to a voltage drift phenomenon in the middle capacitor. By regulating the voltage of the middle capacitor at the rated value, the rest two capacitor voltages can also be maintained at their nominal values.

From (8), the average value of I_{J-} can be regulated by adjusting the reference voltage. One of the most common methods for modifying the phase-voltage reference is to inject a zero-sequence voltage component. To ensure that the line-to-line output voltage is not altered while preserving three-phase voltage symmetry, the ZSV design should satisfy the following constraint:

(1) The offset voltage frequency must be three times the fundamental frequency.

(2) The interval [$\pi/3$, $2\pi/3$] contains the ZSV's effective area.

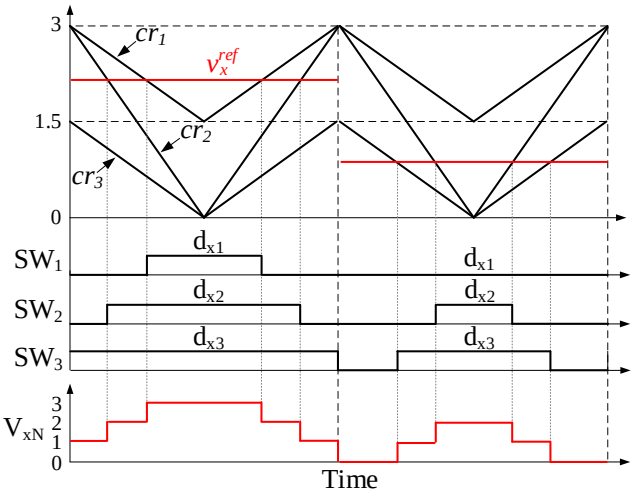


Fig. 4. COPWM modulation scheme for 4L π-Type.

To reduce I_{J-}, the zero-sequence voltage (ZSV) should be designed such that the reference signal of a phase voltage is either 0 or 3. Conversely, to increase I_{J-}, the ZSV should be selected to keep the phase voltage clamps at voltage level of E or 2E. To maximize the average current I_{J-}, the offset component should be adjusted such that the new reference signal becomes 1 or 2 within the interval [π/3,2π/3]. Conversely, to minimize I_{J-}, the new reference signal should be 0 or 3 when θ lies in [π/3,2π/3]. The value of I_{J-} can be regulated within its allowable upper and lower limits by varying the active interval of the injected ZSV. Fig. 3 illustrates the reference voltages obtained after ZSV injection.

2.3. COPWM-Based Voltage-Balancing Method

Although ZSV injection enables capacitor-voltage balancing under LSPWM, I_{J-} can no longer be forced to zero using the balancing offset signal at higher modulation indices. This occurs because both the upper and lower limits of I_{J-} remain positive. Consequently, the PWM method is

switched to a COPWM, which can accomplish natural voltage-balancing capabilities over the entire operation range, in order to balance capacitor voltages at high modulation index [19], [20].

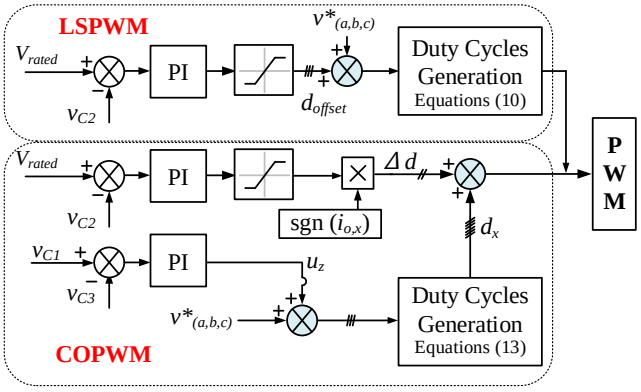


Fig. 5. Block diagram for capacitor voltage control.

Table 2. Simulation parameters

Parameter	Symbol	Value
Rated power	S_{rated}	3 kVA
DC input voltage	V_{dc}	300 V
DC-link capacitance	C_0	2 mF
Carrier frequency	f_{sw}	5 kHz
Output line voltage	$V_{l\text{-}l}$	210 V
Output frequency	f_o	50 Hz
Resistive–inductive load		15 Ω/PF = 0.95

According to Fig. 4, the duty cycles of $SW_{1,x}$, $SW_{2,x}$, and $SW_{3,x}$ are written as follows.

$$\begin{cases} d_{x1}=\dfrac{2v_x^{ref}-3}{3};\ d_{x2}=\dfrac{v_x^{ref}}{3};\ d_{x3}=1 & \left[1.5\le v_x^{ref}<3\right] \\ d_{x1}=0;\ d_{x2}=\dfrac{v_x^{ref}}{3};\ d_{x3}=\dfrac{2v_x^{ref}}{3} & \left[0\le v_x^{ref}<1.5\right] \end{cases} \quad (13)$$

By substituting (13) into (7) and (8), the combined and differential junction currents within one sampling interval can be obtained as:

$$I_{j+}=\sum_{x=a,b,c}\begin{cases}(1/3)\cdot\left(-2v_x^{ref}+6\right)\cdot i_{0,x} & \left[1.5\le v_x^{ref}<3\right] \\ (1/3)\cdot\left(2v_x^{ref}\right)\cdot i_{0,x} & \left[0\le v_x^{ref}<1.5\right]\end{cases} \quad (14)$$

$$I_{j-}=\sum_{x=a,b,c}\begin{cases}0 & \left[1.5\le v_x^{ref}<3\right] \\ 0 & \left[0\le v_x^{ref}<1.5\right]\end{cases} \quad (15)$$

From (14) and (15), both currents have zero average values over one fundamental period under balanced sinusoidal operating conditions, resulting in zero net junction current. However, without proper regulation under nonideal or transient conditions, voltage imbalance may occur. Therefore, when the top and bottom capacitor voltages vary within one sampling interval, a total-junction-current reference should be introduced into J_1 and J_2. Fig. 5 shows the capacitor-voltage control block diagram.

3. SIMULATED RESULTS AND COMPARISON

To demonstrate the effectiveness of the PWM method and capacitor-voltage controller, simulations were carried out using PSIM. The simulation parameters of the inverter are summarized in Table 2.

Figs. 6 and 7 illustrate the waveforms of the capacitor voltages, phase reference and output voltages, line voltage, and output current under LSPWM operation for modulation indices of 0.5 and 0.7, respectively. When m = 0.5, the capacitor voltages are effectively regulated using the proposed ZSV injection method. However, at a modulation index of 0.7, this balance is disrupted.

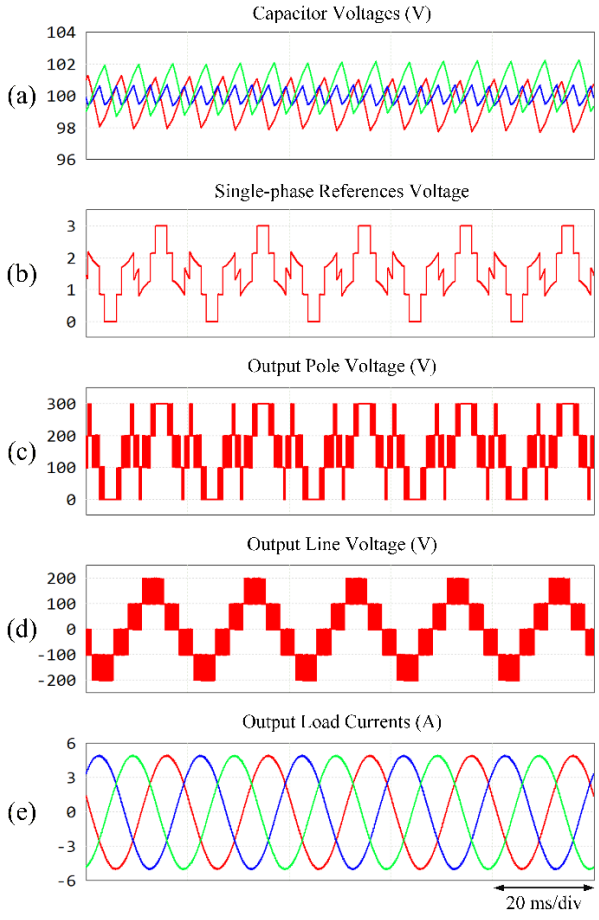


Fig. 6. Performance under LSPWM scheme at m = 0.5.

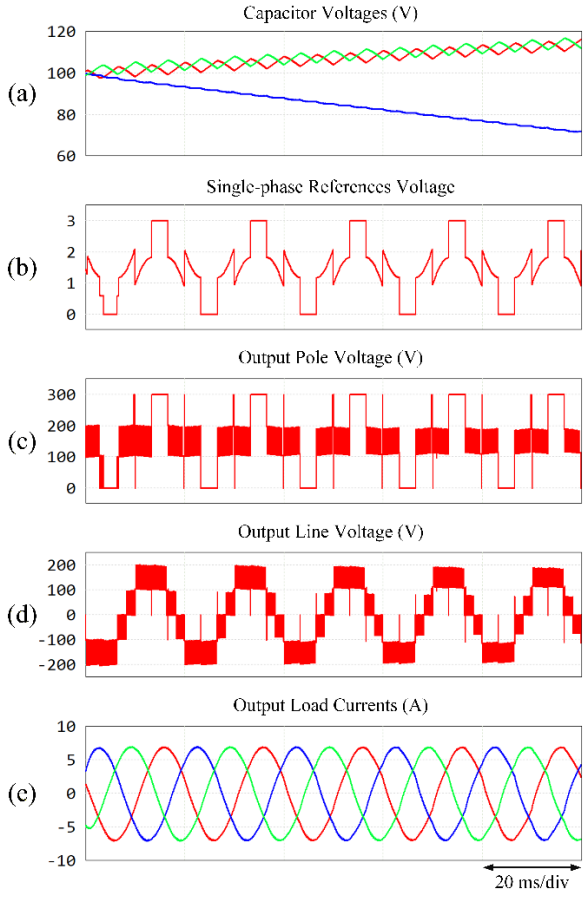


Fig. 7. Performance under LSPWM scheme at m = 0.7.

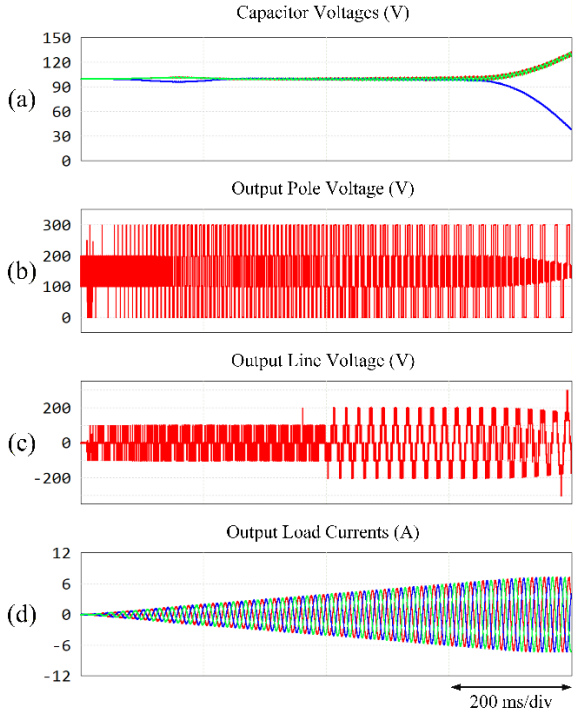


Fig. 8. Performance under LSPWM with a gradually increasing modulation index.

To determine the boundary of LSPWM with capacitor voltage balancing capability, the result of a steadily increasing modulation index is shown in Fig. 8. Starting from 0, the modulation index is gradually raised. As indicated in Table 2, the proposed LSPWM-based balancing method is limited to m = 0.5 for high-PF load conditions, as the NP voltages start to deviate from their balanced values at 0.5 s. This result aligns with the theoretical framework presented in [15].

The performance of the COPWM-based voltage-balancing method operation (m = 0.9) is illustrated in Fig. 9. The well-regulated three DC-link capacitor voltages confirm the effectiveness of the voltage controller under the COPWM scheme in high-modulation-index regions.

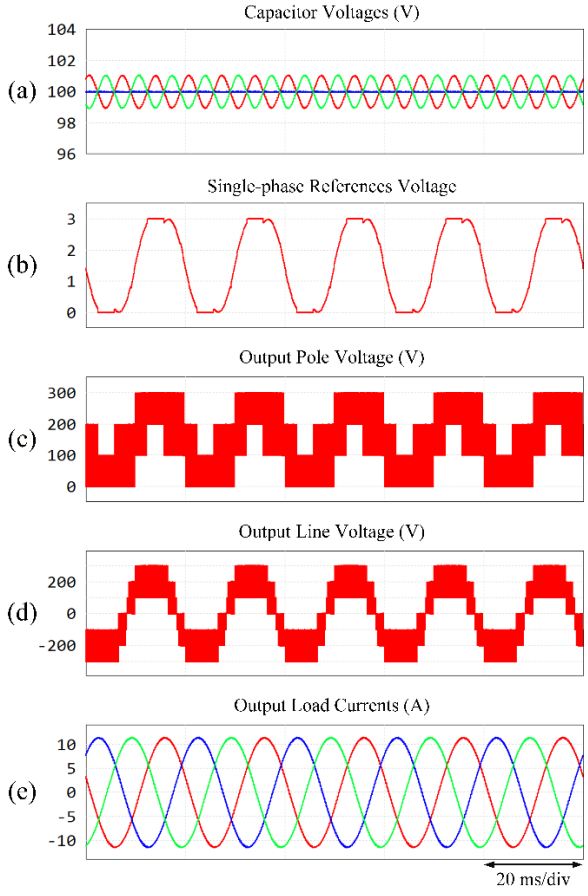


Fig. 9. Performance under COPWM scheme at a modulation index of 0.9.

To ensure capacitor-voltage regulation over the full modulation-index range, the hybrid PWM modulation approach combines LSPWM and COPWM for different modulation indices. The LSPWM-based voltage balancing technique is employed to reduce switching losses and improve THD at low modulation indices (< 0.5). For high modulation indices (> 0.5), the COPWM technique regulates the capacitor voltages. Fig. 10 shows the inverter output characteristics during variable voltage and frequency

with the hybrid PWM strategy. The regulation of all capacitor voltages at their rated values demonstrates the effectiveness of the proposed PWM approach.

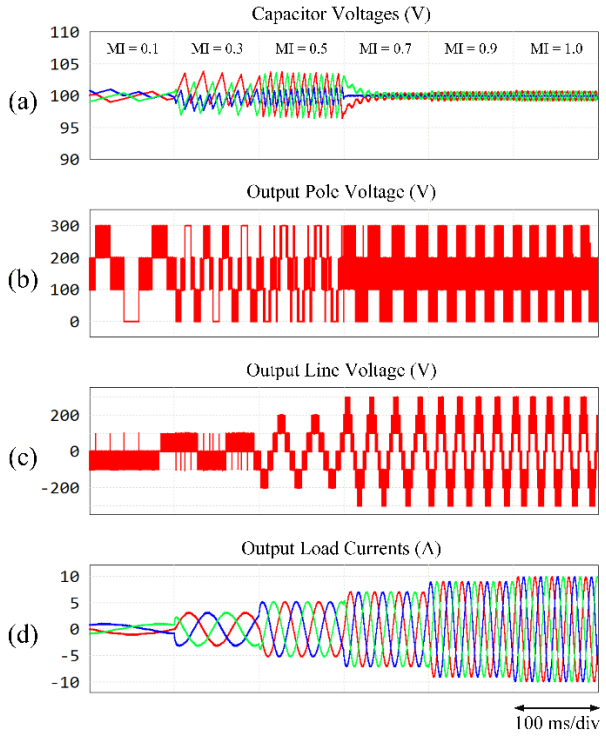


Fig. 10. Performance during VVVF operation.

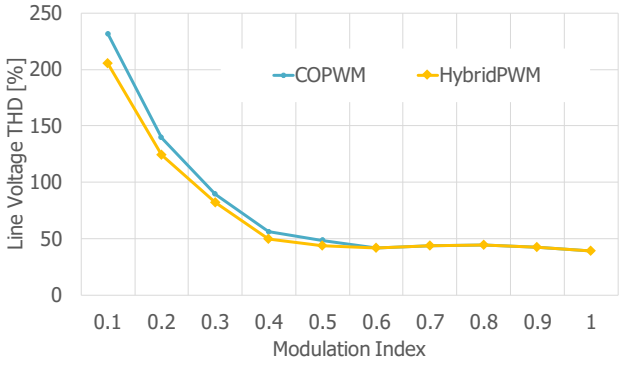


Fig. 11. Comparison of line voltage THD between COPWM and hybrid PWM.

A comparative evaluation of the proposed hybrid PWM and COPWM confirms the superiority of LSPWM over COPWM in reducing switching losses and THD in the low modulation index range, as shown in Fig. 11. Fig. 12 shows the total switching transitions for the inverter under COPWM and LSPWM when m = 0.5. LSPWM results in approximately 4000 switching transitions in the first second, less than 5000 of the 5 kHz carrier frequency due to ZSV clamping. In contrast, COPWM causes around 10,000 transitions, twice the carrier frequency. This demonstrates that COPWM has more switching transitions than LSPWM. Additionally, Fig. 13 highlights that LSPWM has lower switching losses than COPWM at low modulation indices.

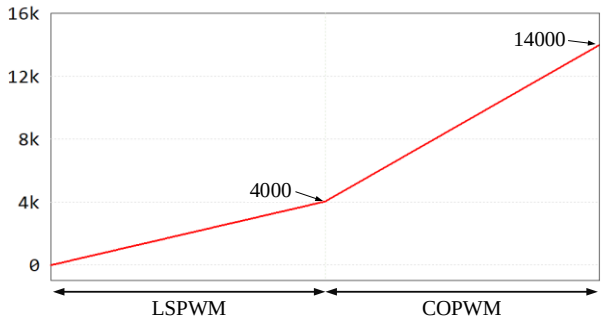


Fig. 12. Switching transition count of LSPWM and COPWM at m = 0.5.

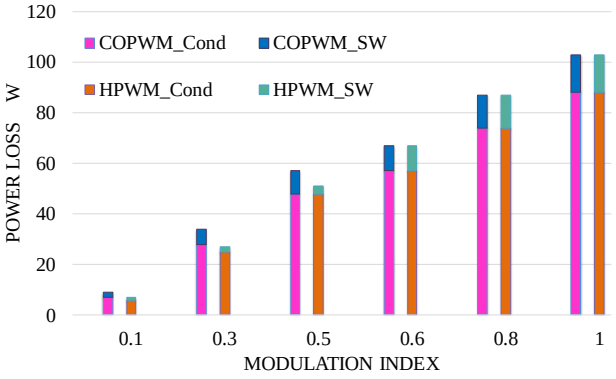


Fig. 13. Power loss comparison in various Mis between COPWM and Hybrid PWM at PF = 0.95.

4. CONCLUSIONS

This study proposes a hybrid PWM technique for the four-level π-type inverter, integrating COPWM and LSPWM to optimize performance across different modulation index ranges. LSPWM is utilized at low modulation indices for capacitor voltage balancing, while COPWM is applied at higher indices for automatic voltage regulation.

Capacitor voltage balancing controls are designed for each PWM method. This hybrid approach, along with the voltage controller, maintains the DC-link capacitors at their nominal values throughout the entire operating range. At lower modulation indices, LSPWM effectively reduces switching losses and total harmonic distortion (THD) compared to COPWM. Simulation results from a 3-kVA inverter prototype confirm the effectiveness and potential of the hybrid PWM method in enhancing inverter performance.

REFERENCES

[1] De S, Banerjee D, Siva Kumar K, Gopakumar K, Ramchand R, Patel C. 2011. Multilevel inverters for low-power application. IET Power Electronics (4): 384-392.

[2] Kouro S, Malinowski M, Gopakumar K, Pou J, Franquelo

LG, Wu B, Rodriguez J, Pérez MA, Leon JI. 2010. Recent advances and industrial applications of multilevel converters. IEEE Transactions on industrial electronics (67): 2553-2580.

[3] Zhang X, Zhao T, Mao W, Tan D, Chang L. 2018. Multilevel inverters for grid-connected photovoltaic applications: Examining emerging trends. IEEE Power Electronics Magazine (5): 32-41.

[4] Bana PR, Panda KP, Naayagi RT, Siano P, Panda G. 2019. Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation. IEEE ACCESS (7): 54888-54909.

[5] Bughneda A, Salem M, Richelli A, Ishak D, Alatai S. 2021. Review of multilevel inverters for PV energy system applications. Energies (14): 1585-1608.

[6] Harbi I, Rodriguez J, Poorfakhraei A, Vahedi H, Guse M, Trabelsi M, Abdelrahem M, Ahmed M, Fahad M, Lin CH, Wijekoon T. 2023. Common DC-link multilevel converters: topologies, control and industrial applications. IEEE Open Journal of Power Electronics. (4): 512-538.

[7] Van TL. 2024. A hybrid cross-connected modular multilevel converter for medium-voltage variable-speed motor drives. GMSARN International Journal (18): 278-284.

[8] Thanh NP, Hai QT, Anh TV. 2024. An Improved PWM Technique for Two-Level Quasi Switch Three-Phase Boost Converter. GMSARN International Journal (18): 1-8.

[9] Yuan X. 2015. A four-level π-type converter for low-voltage applications. In 2015 17th European Conference on Power Electronics and Applications. Geneva, Switzerland, Sep 8: 1-10.

[10] B. Jin and X. Yuan. 2019. Topology, Efficiency Analysis, and Control of a Four-Level π -Type Converter. IEEE Journal of Emerging and Selected Topics in Power Electronics (7): 1044–1059.

[11] Rodriguez J, Bernet S, Steimer PK, Lizama IE. 2009. A survey on neutral-point-clamped inverters. IEEE transactions on Industrial Electronics (57): 2219-2230.

[12] Wu M, Li YW, Konstantinou G. 2020. A comprehensive review of capacitor voltage balancing strategies for multilevel converters under selective harmonic elimination PWM. IEEE Transactions on Power Electronics (36): 2748-2767.

[13] Saeedifard M, Iravani R, Pou J. 2007. Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter. IEEE Transactions on Industrial Electronics (54): 3255-3266.

[14] Busquets-Monge S, Alepuz S, Bordonau J, Peracaula J. 2008. Voltage balancing control of diode-clamped multilevel converters with passive front-ends. IEEE Transactions on Power Electronics (23): 1751-1758.

[15] Pou J, Pindado R, Boroyevich D. 2005. Voltage-balance limits in four-level diode-clamped converters with passive front ends. IEEE Transactions on Industrial Electronics (52): 190-196.

[16] Pan Z, Peng FZ. 2009. A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters. IEEE Transactions on Industry Applications (45): 1028–1034.

[17] Le QA, Lee DC. 2016. A novel six-level inverter topology for medium-voltage applications. IEEE Transactions on Industrial Electronics (63): 7195-7203.

[18] Dao ND, Lee DC. 2018. Operation and control scheme of a five-level hybrid inverter for medium-voltage motor drives. IEEE Transactions on Power Electronics (33): 10178-10187.

[19] Wang K, Zheng Z, Li Y. 2018. A novel carrier-overlapped PWM method for four-level neutral-point clamped converters. IEEE Transactions on Power Electronics (34): 7-12.

[20] Wang K, Zheng Z, Xu L, Li Y. 2020. A generalized carrier-overlapped PWM method for neutral-point-clamped multilevel converters. IEEE Transactions on Power Electronics. (35):9095-9106.